Influence of Scribe Lane Structures on Wafer Potentials and Charging Damage

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Abstract

Results are presented which show that scribe lane structures can exert a significant influence on surface-substrate potentials and J-V characteristics measured on a wafer surface in plasma and ion-implant processes. The implications of this phenomenon for comparison of charging damage results obtained with charging test vehicles and product wafers are also discussed.

I. Introduction

Considerable progress has been made during the last two decades in the understanding of plasma process induced damage in IC manufacturing. Early observations pointed to plasma non-uniformity as the root cause of damage [1]. This led to improvements in process tools, significantly reducing the importance of *global* plasma non-uniformity as the root cause of the problem. Next, observations of damage in dense, sub-micron patterns led to the realization that *local* imbalance of ion and electron fluxes at the bottom of patterned features could also cause device damage. Countless papers have confirmed this "electron shading" effect and its fundamental nature [2].

Still, the frequent lack of correlations between damage monitors and product yields continue to nurture skepticism in IC fabs that perhaps not all mechanisms contributing to charging damage have been identified. Evidence suggesting this was observed in oxide etcher experiments using CHARM®-2 wafers covered with patterned resist [3,4]. The elevated potentials observed on the resist-covered CHARM®-2 wafers could not be attributed to the "electron shading" mechanism due to the large feature sizes used in the resist patterns.

In this paper evidence is presented which suggests that scribe lane structures routinely used for process control in IC manufacturing may exert significant influence on the surface-to-substrate potentials observed within a die during IC processing, thereby increasing or decreasing the likelihood of device damage.

II. Experimental results

Two types of CHARM®-2 wafers were exposed to plasma and ion implant processes. One type contained a variety of scribe-lane process control structures, the other did not. The CHARM®-2 chip layouts were identical on both wafers. Figure 1 shows the positive potentials obtained in one plasma tool obtained with a CHARM®-2 wafer containing scribe-lane structures. Figure 2 shows the results obtained with a CHARM®-2 wafer without scribe-lane structures. The maximum positive potentials recorded in Figure 1 are 10V, while the corresponding potentials recorded in Figure 2 are 3.3V. The corresponding positive J-V plots are shown in Figures 3 and 4.

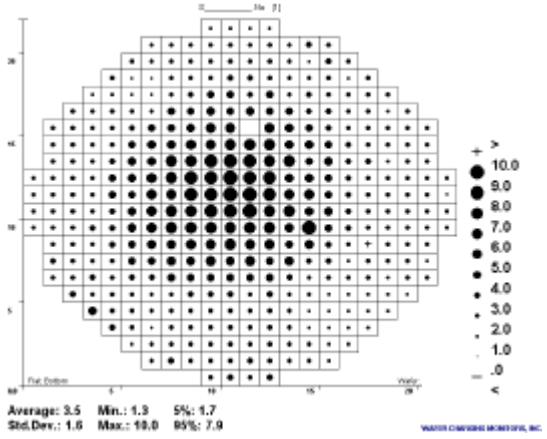

Figure 1. Positive potentials recorded in a plasma tool with a bare CHARM®-2 wafer containing scribe-lane process control structures.

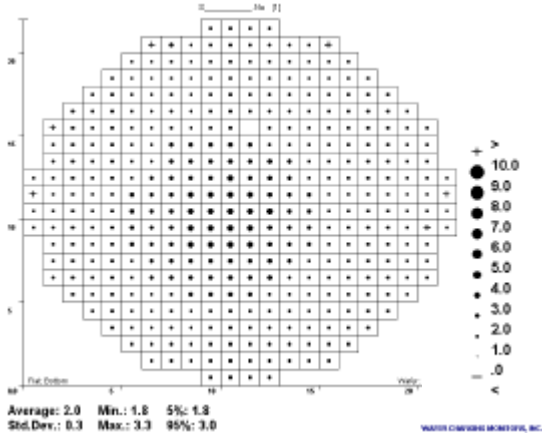

Figure 2. Positive potentials recorded in a plasma tool with a bare CHARM®-2 wafer without scribe-lane process control structures.

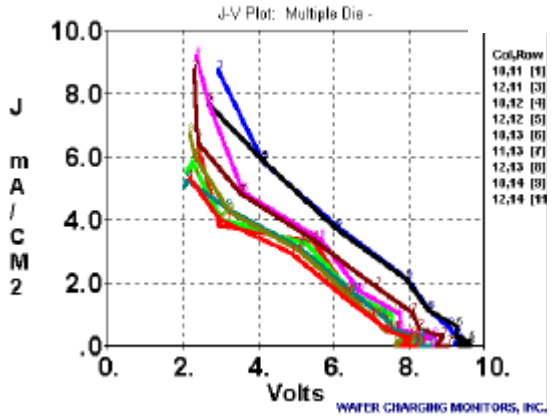

Figure 3. Positive J-V plots recorded in the center of a bare CHARM®-2 wafer containing scribe-lane process control structures.

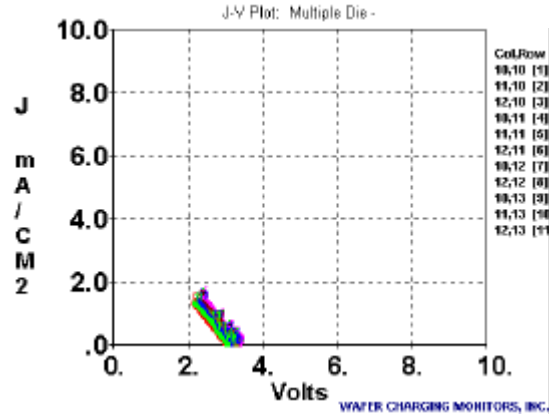

Figure 4. Positive J-V plots recorded in the center of a bare CHARM®-2 wafer without scribe-lane process control structures.

Since the two different CHARM®-2 wafers were manufactured on two different processing lines, the experiment also included one wafer of each type with the residual backside layers removed. This was done to ensure that the back sides of the two wafers were identical. The positive potentials obtained with these wafers were nearly the same as their counterparts obtained on wafers with backside layers intact – less than one volt higher than the results shown above – indicating that the scribe lane differences dominated the differences in the responses shown in Figures 1-4.

A similar experiment was performed in a high-current ion implanter. Both wafer types were implanted with 80 KeV, Arsenic at a beam current density of 0.95 mA/cm^2. The positive potentials obtained with the wafer containing scribe-lane structures are shown in Figure 5, whereas Figure 6 shows the results obtained with the wafer without scribe-lane structures. The results are *opposite* to those obtained in the plasma tool – the positive potentials obtained with the wafer containing scribe-lane structures are on the average 3 V *lower* than the potentials obtained with the wafer without scribe-lane structures. (The peak potentials in both figures are saturated, so comparing peak potentials is not valid.) Similar experiments performed under different implant conditions show that the difference in results obtained with the wafer containing scribe lane structures vs. the wafer without scribe lane structures becomes smaller when the magnitudes of the charging potentials become smaller.

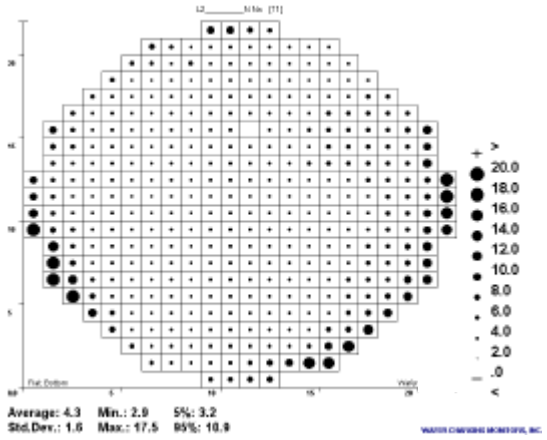

Figure 5. Positive potentials recorded in a high-current ion implanter with a bare CHARM®-2 wafer containing scribe-lane process control structures.

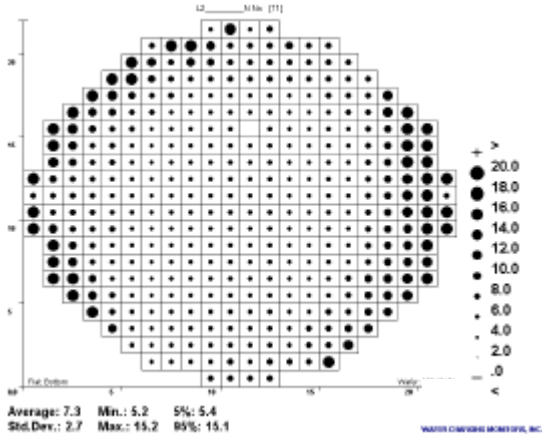

Figure 6. Positive potentials recorded in a high-current ion implanter with a bare CHARM®-2 wafer without scribe-lane process control structures.

III. Discussion of experimental results

The results presented above should not be surprising. The magnitude of surface-substrate potentials experienced by device structures on a wafer results from the interaction between the *entire* wafer and the process environment. Structures of interest are not the only ones responsible for the observed influence. Their neighbors may also exert an influence due to their

connections to the substrate, which may modulate the substrate potential, thereby modulating the surface-substrate potentials.

IV. Implications of experimental results

The results reported here have many implications for the comparison of charging damage results obtained with different, or even the same, test vehicles and products.

These results suggest that:

1. Two wafers possessing the same product or test chip layout may experience different amounts of charging under identical process conditions, unless the masks used to fabricate them also possess identical scribe lane structures. (Scribe lane structures are typically inserted into the mask data base by a manufacturing CAD group, and thus are typically out of control of the product or test chip designer.) Consequently, even results from "standard" layout test chips may contain differences due to the unknown influence of different scribe lane configurations.

2. Comparison of charging results obtained with identical structures embedded in different test vehicles may be even less precise than results obtained with mask sets that differ only in scribe lane structure, due to the unknown influence of both the scribe lane structures and the other test structures.

3. Comparison of charging results obtained with different test vehicles – particularly short-loop test vehicles and product chips whose device content and scribe lanes are very different – is likely to continue being difficult.

However, these comments do not imply that test vehicles, and the results obtained with them, are useless. On the contrary, charging monitors are likely to provide useful information, provided that:

1. The results obtained with charging monitors are used for *relative* comparisons between different processes implemented on the same tool, or tools of similar design, and that the same *mask* set is used for all wafers being compared.

2. The charging monitors, including their scribe lanes, are properly *optimized* for different tool types to obtain a sufficient response. This particularly applies to damage vehicles, whose structures require sufficiently high voltages to cause charge injection into gate oxide to register damage. The requirements for SPORT or CHARM®-2 are less stringent, as long as the signal is sufficiently large to be measured.

These findings also suggest significant implications for equipment manufacturers who use test chips and short-flow monitors to validate performance of their tools:

1. Multiple test chips/vehicles should be used to ensure that a tool performs properly over a range of different layouts and scribe lane configurations that may be encountered in the manufacture of different products.

2. The device content and scribe lane configurations of test chips/vehicles used for this purpose must be properly optimized to obtain sufficient (preferably maximum) responses from the particular tool type. This is especially important for short-loop monitors.

Finally, the results presented in this paper imply that charging models and charging simulation tools need to take into consideration the *entire wafer*, not just isolated structures. Comprehending wafer-scale interaction with the charging environment is essential to achieving better understanding of the influence of different structures (and scribe lanes) on the substrate potential and charging damage. Such understanding will allow us to design better test vehicles and suitably tailor scribe lane structures to minimize surface-substrate potentials, thus minimizing the likelihood of charging damage to product device structures during IC manufacturing.

V. References

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