Charging on Resist-Patterned Wafers during High-Current Ion Implants

Wes Lukaszek[1], Sonu Daryanani[2] and Jeffrey Shields[2]
[1]Wafer Charging Monitors, Inc., 127 Marine Road, Woodside, CA, 94062 USA
[2]Microchip Technology Inc., 1200 South 52nd Street, Tempe, AZ, 85281 USA

***Abstract*-Charging characteristics of As^+ and BF_2^+ high-current ion implants were measured using bare and resist-covered CHARM®-2 wafers patterned with a six-field mask containing holes ranging from 2 um to 0.5 um (as well as clear and resist-covered fields). The results show surprising differences in the charging characteristics of high-current ion implanters compared to contemporary plasma-based process tools. In plasma tools, the "electron-shading" effects increase positive (and decrease negative) potentials and current densities as hole size decreases. On the contrary, high-current ion implants exhibited positive and negative potentials independent of hole size. The positive and negative current densities were also independent of hole size (but significantly higher than in the clear field). These results indicate that charging damage in high-current ion implanters should not increase when implant mask features are scaled down (other factors being equal). We also explain the apparent absence of damage in contemporary high-current ion implanters in spite of the very high positive current densities and high positive potentials.**

I. INTRODUCTION

The presence of photoresist on wafers profoundly affects wafer charging during high current ion implants, and the device damage associated with it. Although significant observations about this were made in early studies which used "antenna" capacitors as detectors [1], understanding of the physical mechanisms ultimately came from the use of the EEPROM-based CHARM®-2 monitors, which allow in-situ measurements of peak positive potentials, peak negative potentials and peak charge-fluxes experienced by device structures on the surface of a wafer [2]. Early experiments with CHARM®-2 monitors covered with uniform [3] and patterned resist films [4] showed large increases in positive charging associated with the presence of resist on CHARM®-2 sensors during high current ion implants. Experiments employing resist layout types used on CMOS product wafers [5] confirmed the large increases in positive charging in the presence of resist patterned with a dark-field mask [6]. However, the resist feature sizes were on the order of 100s of microns, which are significantly larger than contemporary device design rules. The purpose of the present work was to quantify charging phenomena associated with resist patterns using contemporary feature sizes. Moreover, since contemporary ion implanters use plasma flood systems[1], another purpose of this experiment was to compare the ion implant results with results obtained in plasma tools, to see if theories developed to explain charging associated with small feature sizes in plasma tool are applicable to high-current ion implanters.

II. EXPERIMENTAL PROCEDURES

CHARM®-2 wafers, patterned with 1.2µm resist using a six-field resist mask, were implanted in the AMAT 9500 high-current ion implanter. In one field, the resist was completely removed from the entire die. In another field, the resist completely covered the entire die. In the remaining four fields, the resist covered the entire die, but holes were patterned on the charge-collection electrodes (antennas) of the potential and charge-flux sensors using 2µm, 1.5µm, 1µm, and 0.5µm design rules. The wafers were exposed to standard As^+ and BF_2^+ implants. Un-patterned (bare) CHARM-2 wafers, placed on the opposite side of the wheel, were used with each implant as implant monitors.

The first round of experiments compared As^+ and BF_2^+ implants. The As^+ implant (As1) was 80 KeV, 2e15/cm^2, at a beam current of 10 mA and peak current density of 0.48 mA/cm^2. The BF_2^+ implant was 50 KeV, 2e15/cm^2, at a beam current of 6.5 mA and peak current density of 1.26 mA/cm^2. The flood gun was set to arc current of 4 A, and 1.2 sccm of Ar for both implants. The arc voltage was 30 V, and the guide tube voltage was -10 V.

Since qualitatively similar results were obtained for both As^+ and BF_2^+ implants, the second round of experiments compared 80 KeV, 2e15/cm^2 As^+ implants performed at two different flood settings. One implant (As2) was performed at a beam current of 10 mA, peak current density of 1.09 mA/cm^2, and flood arc current of 2 A. The other implant (As3) was performed at the same beam current, peak current density of 1.15 mA/cm^2, and flood arc current of 5 A.

Unless indicated otherwise, the J values in the J-V plots shown later were obtained by dividing the collected currents by the area of the resist openings. Consequently, the J values represent the positive or negative current densities measured in the resist holes. The J-V graphs show J-V plots from the same field over the entire wafer.

III. EXPERIMENTAL RESULTS

The positive J-V plots obtained from the As1 implant are shown in Figures 1a-1f. Figures 1c-1f are nearly identical, indicating that the positive current density is independent of the size of the hole.

[1] Even in when plasma flood is not used, the impact of the ion beam with background gases generates a weak plasma.

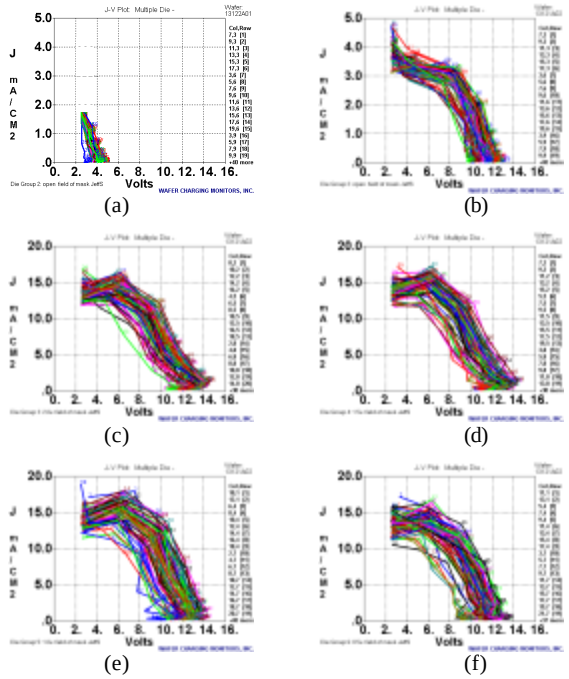


Figure 1. Positive J-V plots recorded during the As1 implant: (a) bare monitor wafer; (b) open field on patterned wafer; (c) 2µm holes; (d) 1.5µm holes; (e) 1µm holes; (f) 0.5µm holes. [Note different J scales in (a) and (b) vs. (c), (d), (e), and (f).]

The corresponding set of negative J-V plots obtained from the As1 implant is shown in Figures 2a-2d. Figures 2c-2d are nearly identical, indicating that the negative charging is also independent of the size of the hole.

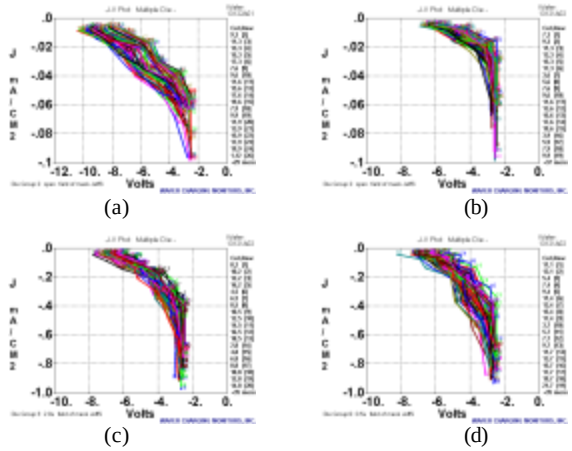


Figure 2. Negative J-V plots recorded during the As1 implant: (a) bare monitor wafer; (b) open field on patterned wafer; (c) 2µm holes; (d) 0.5µm holes. [Note different J scales in (a), (b) vs. (c), (d).]

Similar results were obtained from the BF_2^+ implant. To illustrate the magnitude of positive charging, we show in Figures 3a-3b only the results from the "open" field and the 2um holes field.

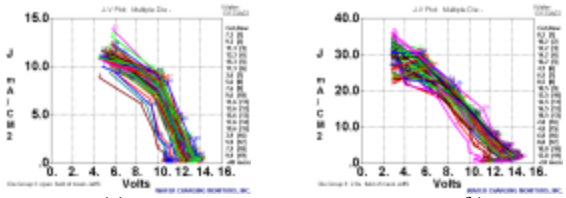


Figure 3. Positive J-V plots recorded during the BF_2^+ implant: (a) open field on patterned wafer; (b) 2µm holes. [Note different J scales in (a) vs. (b).]

The corresponding negative J-V plots for the BF_2^+ implant are shown in Figures 4a-4b.

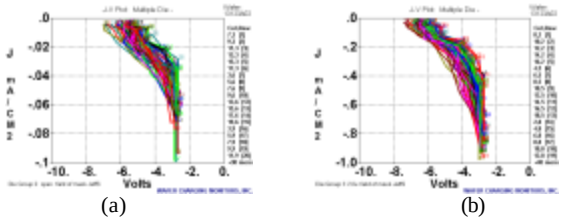


Figure 4. Negative J-V plots recorded during the BF_2^+ implant: (a) open field on patterned wafer; (b) 2µm holes. [Note different J scales in (a) vs. (b).]

The influence of flood on the positive charging characteristics is shown in Figures 5a-b, and Figures 6a-b. Figures 5a-b show the results from the As2 implant (low flood case). The J-V plots are shifted to very high voltages, causing the charge-flux sensors to reach their saturation voltage (~ 16V), which truncated the J-V plots at that voltage.

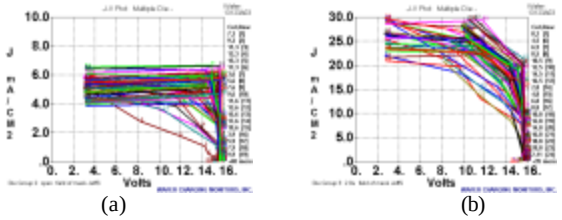


Figure 5. Positive J-V plots recorded during the As2 (low flood) implant: (a) open field on patterned wafer; (b) 2µm holes. [Note different J scales in (a) vs. (b).] Charge-flux sensors are saturated at ~16V, truncating the J-V plots.

Figures 6a-b show the results from the As3 implant (moderately high flood case).

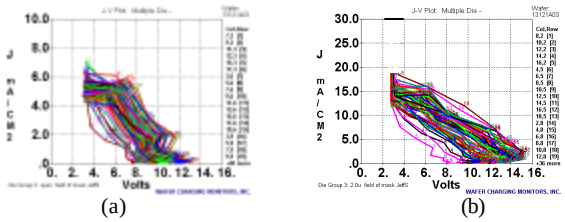
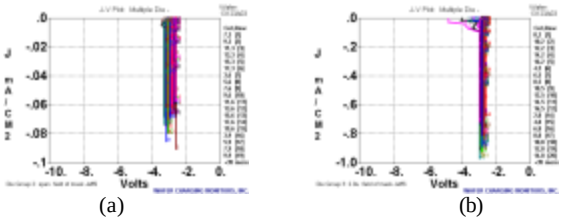


Figure 6. Positive J-V plots recorded during the As3 (high flood) implant: (a) open field on patterned wafer; (b) 2µm holes. [Note different J scales.]

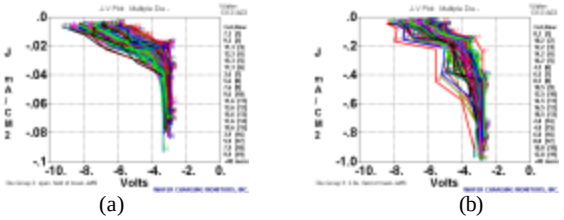
The influence of flood on the negative charging characteristics in shown in Figures 7a-b and Figures 8a-b for the same implants. Figures 7a-b show the results from the As2 implant (low flood case).



(a) (b)

Figure 7. Negative J-V plots recorded during the As2 (low flood) implant: (a) open field on patterned wafer; (b) 2μm holes. [Note different J scales in (a) vs. (b).] The vertical lines in (a) and (b) indicate no response.

Figures 8a-b show the results from the As3 implant (moderately high flood case).

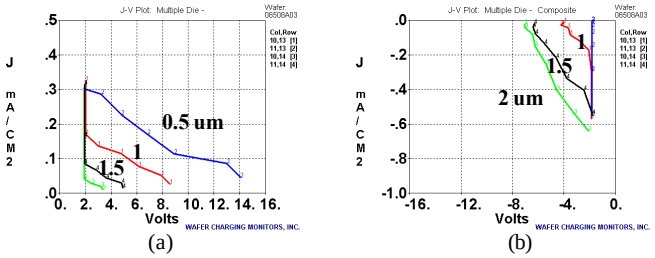


(a) (b)

Figure 8. Negative J-V plots recorded during the As3 (high flood) implant: (a) open field on patterned wafer; (b) 2μm holes. [Note different J scales in (a) vs. (b).]

IV. Discussion of Results

The most striking observation from these experiments is that both positive and negative current densities measured in the resist holes are independent of the size (or, equivalently, the aspect ratio) of the holes. This is completely different from what is observed in plasma tools, which show a strong increase in positive charging (and a strong decrease in negative charging) with decreasing hole size [7]. Example J-V plots, obtained in a non-uniform plasma tool (which would most resemble a high-current ion implanter), using the same resist patterns, are shown in Figures 9a-b.



(a) (b)

Figure 9. J-V plots for 2μm, 1.5μm, 1μm, and 0.5μm holes obtained in a non-uniform plasma oxide etcher. (a) positive J-V, (b) negative J-V.

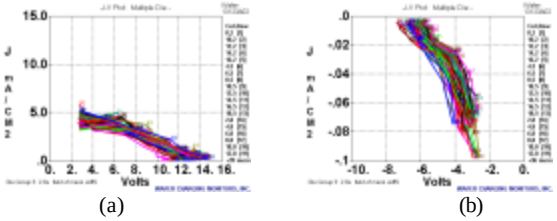
Comparison of the results shown in Figure 9, which are characteristics of plasma tools used in wafer manufacturing, and the ion implant results presented here, makes it very clear that even a plasma flood equipped ion implanter behaves very differently from a plasma tool.

This is a welcome finding, since it indicates that charging damage problems in high-current ion implanters will not get worse as feature sizes decrease with continued device scaling. Although high positive potentials are generated during a low-flood implant, as shown in Figure 5b, increasing flood brings them down, as shown in Figure 6b, to a level where the depletion layers under n-channel devices, and reverse-biased N-well junctions under p-channel devices, can prevent positive current flow through gate oxides [8] – which could otherwise become problematic due to the very large positive current densities. Moreover, as shown in Figure 8, the increased flood required to do this does not generate high negative current densities which could damage n-channel devices. Although the negative potentials are sufficient to inject current into contemporary gate oxides, the low-level damage caused by negative charging will be annealed out during the high-temperature implant activation step.

The difference in charging behavior between plasma tools and ion implanters could be explained as follows. The aspect-ratio dependence of the positive J-V shown in Figure 9a is due to the "electron shading" effect [9], where the upper inside portion of the resist hole becomes charged negative and sets up a potential barrier to entry of electrons which are needed to neutralize the positive ion flux collected at the bottom of the hole. (The reduction of the negative ion flux with increasing aspect ratio is clearly visible in Figure 9b.) However, in the ion implant case, the positively charged resist [3] will collect all secondary electrons produced by the beam at the bottom of the resist hole and repel most of the (low-energy) plasma ions, resulting in a positive current density $J_b(a+\gamma)$, where J_b is the beam current density, a is the beam current neutralization fraction (between 0 and 1), and γ is the secondary electron emission coefficient. This process is independent of feature size (at least for small features).

The remaining discussion will address the shift of the J-V plots along the voltage axis on the bare vs. resist-patterned wafers, and the differences in the J values obtained in the open vs. the resist-patterned fields on the resist-covered wafers.

When the currents densities in the patterned fields are treated as if the entire charge-collection electrode (CCE) is collecting current (which is unreasonable since about 86% of the CCE was covered by resist), the positive and negative J-V plots shown in Figures 10a-b are obtained.



(a) (b)

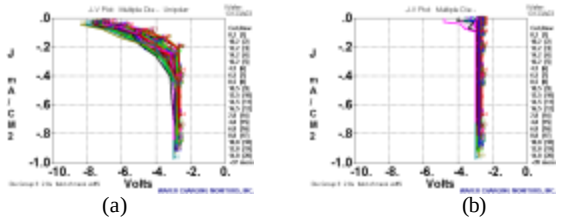
Figure 10. Unscaled J-V plots for 2μm holes (BF_2^+ implant): (a) positive J-V; (b) negative J-V.

Comparison of Figure 10a with Figure 3a confirms that the amount of positive current collected by the 2um holes was, indeed, smaller than the amount of current collected by the uncovered CCE. However, Figure 10b and Figure 4a are virtually the same, indicating that the same amount of negative current was collected with a 86% resist-covered CCE as with a bare CCE.

This observation could help explain the previously reported shift of the positive J-V plots toward higher voltages, and the corresponding shift of the negative J-V plots toward less negative voltages, as the area of charge collection electrodes connected to the substrate is decreased [10], or as most of the area of the wafer is covered with photoresist [6]. Since CCEs appear to be more effective at collecting negative current than positive current, the net effect of decreasing the CCE areas (by covering them with photoresist, or by reducing their size) is to shift the balance of the collected current routed to the substrate in favor of negative current. The substrate is thus biased more negative, thereby increasing the positive surface-substrate potential difference, and decreasing the negative surface-substrate potential difference. This has the effect of shifting the positive J-V plots to higher positive voltages, and shifting the negative J-V plots to less negative voltages. This global effect is apparent in Figure 1a and Figure 1b, vs. Figure 2a and Figure 2b.

A closer look at Figures 10a and 3a, however, reveals a curious discrepancy. Since 86% of the CCE area was covered with resist (in the resist-patterned fields), the unscaled current density shown in Figure 10a should be a factor of 1/0.14 7 lower than in Figure 3a, according to the proposed model. However, a reduction by a factor of ~ 3 is actually observed. This suggests the existence of additional current components, perhaps leakage currents from the positively-charged resist, as previously proposed in [11]. The first set of previous measurements using CHARM-2 wafers suggested this possibility [4], whereas the second set did not [5,6]. However, the resist designs used in the second set of experiments used resist openings on the order of hundreds of microns, which emphasized area effects. The small features used in the current round of experiments were hundreds of times more perimeter intensive, and thus would have been much more sensitive to resist side-wall related (leakage?) phenomena. Additional experiments using resist patterns having different perimeter/area ratios would be necessary to investigate this phenomenon in more detail.

Another peripheral observation made during these experiments was the significant reduction in negative charging at the end of a low-flood implant vs. (most likely) the beginning of the implant. This was observed by comparing the negative J-V plots obtained with the unipolar charge-flux sensors, which respond to peak negative charging, vs. the non-polar charge-flux sensors, which respond to charging at the end of the implant. The effect is shown in Figures 11a-b.



(a) (b)

Figure 11. Negative J-V plots for 2µm holes (As; low flood): (a) beginning; (b) end of implant.

V. CONCLUSIONS

Wafer charging characteristics of high current As^+ and BF_2^+ implants were evaluated using CHARM-2 wafers covered with patterned 1.2µm resist. Positive and negative current densities measured in 2µm, 1.5µm, 1µm, and 0.5µm holes were independent of hole size, in marked contrast to results obtained in plasma tools used in IC processing. Peak positive and negative charging could be controlled with the use of plasma flood[2], indicating that **c**harging damage in high-current ion implanters should not increase when implant mask features are scaled down (other factors being equal).

REFERENCES

[1] R. Tong and P. McNally, "Effect of Resist Patterning on Gate Oxide Integrity in Source/Drain Implant," *Nucl. Instr.in Meth. in Phys. Res. B6,* pp. 376-381, 1985.

[2] W. Lukaszek, Technical Note 1, Wafer Charging Monitors, Inc.

[3] W. Lukaszek, S. Reno, and R. Bammi, "Influence of Photoresist on Wafer Charging During High Current Arsenic Implant," *Proc. XI Intl. Conf. on Ion Impl. Tech.,* pp. 89-92, June 16-21, 1996.

[4] W. Dixon, W. Lukaszek, and C. Heden, "Photoresist-Enhanced Charging During High Current Ion Implant," *Proc. XI Intl. Conf. on Ion Impl. Tech.,*pp. 85-88, June 16-21, 1996.

[5] Lukaszek and M. Current, "Photoresist Mask Design for Evaluation of Resist-Mediated Charging Effects During High Current Ion Implantation," *1998 Intl. Conf. on Ion Impl. Tech. Proc.,* pp.658-661, June 22-26, 1998.

[6] M. Current, M. Foad, S. Brown, W. Lukaszek, and M. Vella, "Photoresist Effects on Wafer Charging Control: Current-Voltage Characteristics Measured with CHARM-2 Monitors During High Current As Implantation," *1998 Intl. Conf. on Ion Impl. Tech. Proc.,* pp. 490-493, June 22-26, 1998.

[7] W. Lukaszek and J. Shields, "Electron Shading Effects During Oxide Etching in Uniform and Non-Uniform Plasmas", *2002 7th Intl. Symp. on Plasma and Process Induced Damage,* pp. 68-71, June 6-7, 2002.

[8] Lukaszek, M. Rendon, and D. Dyer, "Device Effects and Charging Damage: Correlations Between SPIDER-MEM and CHARM-2", *1999 4th Intl. Symp. on Plasma Process Induced Damage,* pp. 200-203, May 10-11, 1999.

[9] K. Hashimoto, "Charge damage caused by electron shading effect," *Jpn. J. App. Phys.*, pp. 6013-6018,1994.

[10] W. Lukaszek, "Influence of Scribe Lanes on Wafer Potentials and Charging Damage," *2000 Intl. Conf. on Ion Impl. Tech. Proc.,* pp. 569-572, Sept. 17-22, 2000.

[11] H. Muto, H. Fujii, K. Nakanishi, and S. Ikeda, "A Mechanism of Gate Oxide Deterioration During As Ion Implantation," *IEEE Trans. El. Dev.,* vol. 38, pp. 1296-1302, June 1991.

[2] Other types of charge-control systems were not evaluated.