HOW TO AVOID CHARGING DAMAGE IN IC MANUFACTURING

Wes Lukaszek
Wafer Charging Monitors, Inc.
127 Marine Road, Woodside, CA 94062 USA

Wafer charging damage during IC processing is the result of complex interactions between the wafer environment and the wafer. Understanding these interactions, and recognizing the relative importance of the different mechanisms capable of causing damage, are essential for successful diagnosis and control of charging damage during wafer manufacturing. This paper presents a unified perspective of charging damage in IC manufacturing, and from it derives a set of guidelines which can be used by equipment and IC manufacturers to avoid charging damage to ICs during wafer processing.

INTRODUCTION

Charging damage during wafer processing is often perplexing, as evident from the countless papers that have been written about it during the last twenty years. However, when we look for the *fundamentals* behind charging damage, we find a single underlying cause: charge trapping in SiO_2 near device space charge regions. This single cause is responsible for *all* of the observed device effects, including threshold voltage shifts, transconductance degradation, enhanced junction leakage, etc. Since charge trapping is a consequence of charge *transport* through the affected SiO_2 regions [1], the *process phenomena responsible for charging damage can be inferred from the basic physical mechanisms governing charge transport in SiO_2*.

The two mechanisms responsible for charge conduction in SiO_2 are: (a) electron tunneling through the SiO_2 potential barrier, illustrated in Figure 1, which requires very high electric fields in the SiO_2 [1], and (b) charge transport over the SiO_2 potential barrier, illustrated in Figures 2a and 2b, which occurs even at low electric fields in the presence of UV light [2]. The mechanism illustrated in Figure 2a, in which electrons from the conduction or valence band of silicon are excited to the conduction band of the SiO_2, and subsequently transported by electric fields in the SiO_2, occurs at photon energies greater than 3.2 eV (388 nm), but lower than ~9 eV (138 nm). At these photon energies, the SiO_2 is transparent to UV, so this mechanism can affect device structures located deep under the surface of the wafer. At photon energies greater than ~ 9 eV, the SiO_2 becomes conductive due to the mechanism shown in Figure 2b, where UV breaks SiO_2 bonds, creating electron-hole pairs. Although photons with energies greater than ~ 9 eV are rapidly absorbed in the SiO_2 and the electron-hole pairs are produced at the surface of the wafer, they become separated and transported to device structures by the electric fields which may be present in the SiO_2.

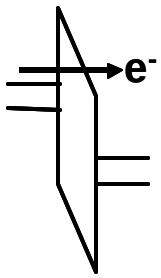
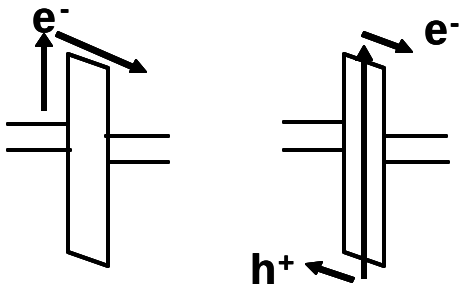


Figure 1. Charge transport at very high electric field (tunneling).



(a) (b)

Figure 2. UV-enabled charge transport: (a) 3.2 eV < h? < 9 eV; (b) h? > 9 eV

Consequently, since surface charging produces the electric fields responsible for charge transport, it is apparent that *in high UV environments surface charging is not acceptable*. In processes where UV intensity is very low, some wafer surface charging may be tolerated, provided it is not sufficient to cause the high electric fields required by the electron tunneling mechanism illustrated in Figure 1.

Regardless of which device parameters are affected, these *are* the underlying basics of charging damage. However, the implications they carry depend on the process tools, processes, and device types in question. We will next discuss processes typically responsible for charging damage.

OXIDE DEPOSITION

During plasma oxide deposition, when the entire wafer surface is exposed to intense UV, even low levels of wafer charging can cause damage. Consequently, plasma oxide depositions are often troublesome processes in wafer manufacturing. Several causes contribute to this. The principal reason for gate oxide damage is the huge reduction in the breakdown charge (Q_{bd}) of the oxide. At the high deposition temperature – typically around 400 ^{o}C – the breakdown charge of the oxide is reduced by several orders of magnitude [3]! This drastically reduces the amount of oxide current that needs to be collected by electrodes connected to transistor gates in order to cause transistor damage. This current is readily supplied by relatively low levels of surface charging when the oxide becomes conductive due to the intense UV.

During the early stage of deposition, when topographical features are prominent on the surface of a wafer, it may be possible that the "electron shading" mechanism (discussed later) also contributes to the observed damage [4]. However, as the deposition proceeds, trenches become filled, reducing the magnitude of this effect. Moreover, this mechanism cannot explain the increase in damage with increasing deposition. Consequently, it is safe to conclude that the primary cause of charging damage during oxide deposition is the UV-enabled conduction mechanism: UV generates the charges that are then transported to different device structures with the help of the electric field established by surface charging. Moreover, it is observed that when surface charging is

eliminated by making the deposition plasma uniform, charging damage is eliminated – even though the intense UV is still present [5].

It should be noted that gate oxide damage is not the only form of device damage possible under these conditions. Other types of damage (i. e., device parameter shifts) are also possible when charges are transported to, and trapped near, device space charge regions. Among them are: increased junction leakage, increased source-drain leakage, beta degradation in bipolar transistors, etc. Consequently, *to avoid charging damage during oxide depositions, surface charging must be completely eliminated*.

EFFECT OF UV AND CHARGING ON NON-VOLATILE ICs

A different symptom of the cooperative effect between UV and surface charging was observed during manufacture of floating-gate non-volatile memory devices [6,7]. Here, charge conduction in SiO_2, caused by UV and elevated positive potentials around wafer periphery, shown in Figure 3a, led to charge trapping on EPROM transistor floating-gates during via etch, equivalent to EPROM programming. During forming gas anneal, the electric field in the SiO_2 surrounding the floating-gates led to the formation of positive traps via the NBTI mechanism [8,9]. The positive traps, in turn, caused charge-loss from the floating gates during charge-storage tests, evident from threshold voltage margin instabilities around wafer periphery, as shown in Figure 3b. The role of UV in this case was unmistakable, since changes in the gas mixture used during the via etch showed a significant influence on UV intensity and the observed charge-loss. By reducing the amount of CO in the gas mixture, it was possible to eliminate the threshold voltage margin instability [6]. At the same time, changes in the gas mixture had no effect on the level of surface charging, so the disappearance of the threshold voltage margin instability was clearly due to change in the spectrum and intensity of UV.

This mechanism was confirmed by programming EPROMs on a tester over the entire wafer, and then subjecting the wafers to a forming gas anneal. All die whose EPROMs were programmed on the tester to a high V_t state failed the threshold voltage margin instability test, as shown in Figure 3c.

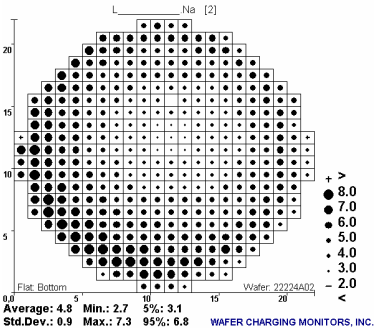


Figure 3a. Positive potentials during via etch.

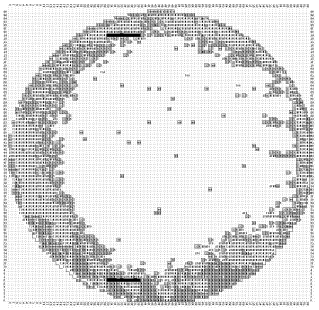


Figure 3b. Die around periphery fail margin tests (black = fail).

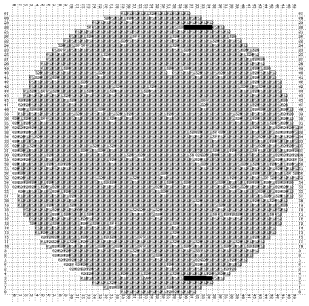


Figure 3c. Programmed die fail margin tests after forming gas anneal.

ETCHING PLASMAS – "ELECTRON SHADING" EFFECT

Plasmas that are uniform[1] over the entire surface of a wafer do not cause surface charging, and thus would appear to eliminate damage from the electron tunneling mechanisms, as well as from the cooperative effect of UV and surface charging. However, during etching, a feature-size-dependent "electron shading" mechanism causes localized charging at the bottom of the holes of etched features [10]. This effect is due to the anisotropic ion flux[2] used in etching plasmas and the isotropic electron flux. As illustrated in Figure 4, the isotropic electron flux charges negatively the inside top of narrow resist holes (or lines) thereby setting up a potential barrier to entry of electrons. Since electrons cannot enter the holes and neutralize the ion flux, positive charging results at the bottom of the resist holes. Conversely, in regions where the resist spacing is wide electrons can enter the holes, setting up a negative potential. The combination of high positive potentials in some regions of a die, and negative potentials in other regions of a die creates the equivalent of an intra-die plasma non-uniformity, causing charge flow through the gate oxides of transistors, thereby creating damage. Making the plasma uniform minimizes this effect, but does not eliminate it, as shown in Figure 5a. However, the intensity of charging due to this mechanism is *greatly* increased in non-uniform plasmas, as illustrated in Figure 5b [11]. Consequently, *etching plasmas must be made uniform to minimize the "electron shading" effect and thus minimize device damage.*

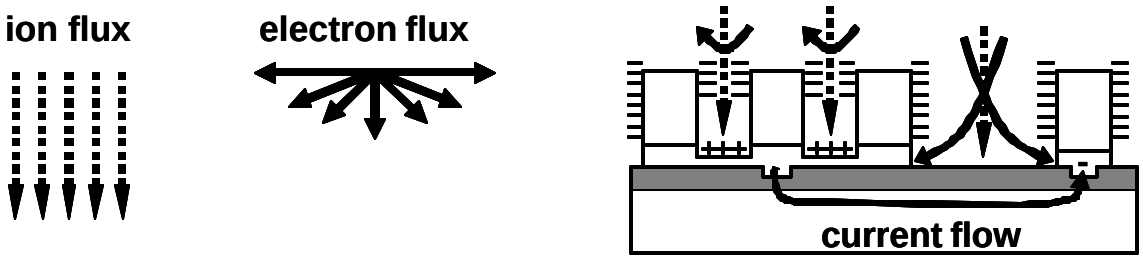


Figure 4. The anisotropic ion flux and isotropic electron flux in etching plasmas cause positive charging at the bottom of narrow trenches, and negative charging at the bottom of wide trenches.

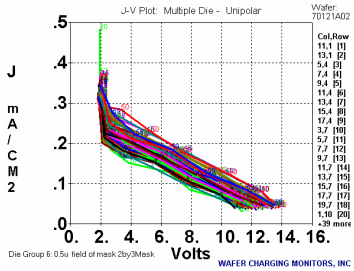


Figure 5a. Uniform plasma produces uniform positive charging over entire wafer in 0.5 um holes (in 1.2 um resist).

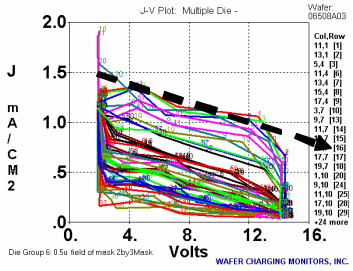


Figure 5b. Non-uniform plasma produces non-uniform, and greatly enhanced, positive charging (note J scale change).

[1] Meaning, that electron and ion fluxes are equal at every point on the wafer.
[2] Produced by the application of RF bias to the wafer.

EFFECT OF SUBSTRATE ANTENNAS

To *prevent* charging damage from "electron shading", the size of charge-collecting "antennas" connected to transistor *gates* is limited during circuit design. However, recent work [12,13,14] indicates that the size of charge-collecting "antennas" connected to wafer *substrate* exerts a significant effect on surface potentials and charging currents sensed by "antennas" connected to transistor gates: the smaller the area of the "antennas" connected to the substrate, the greater the charging experienced by the "antennas" connected to transistor gates, as illustrated in Figure 6. Consequently, in addition to enforcing gate "antenna" design rules, efforts should me made to maximize the area of the "antennas" connected to wafer substrate.

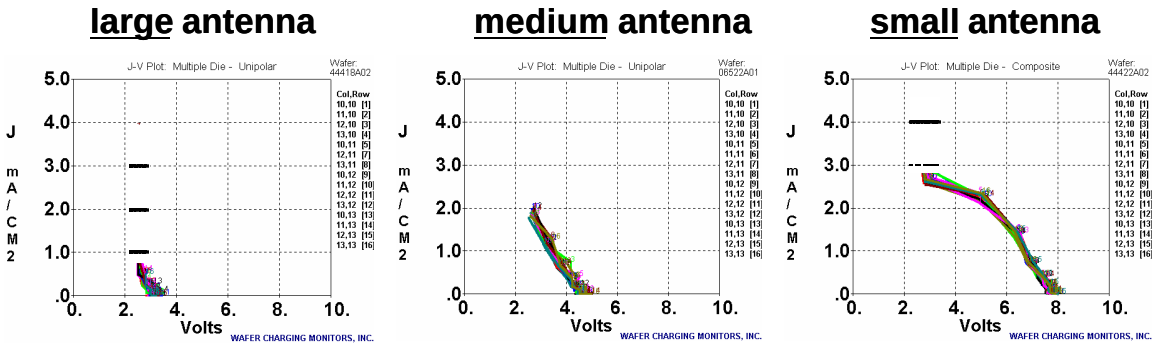


Figure 6. Positive charging measured on identical antennas connected to transistor *gates* increases (J-V plots move to higher voltages) when the size of antennas connected to wafer *substrate* decreases.

ION IMPLANTATION

Control of wafer charging in ion implanters is governed by an entirely different set of rules. Since UV intensity in ion implanters is typically very low, charging damage during ion implantation results only from electron tunneling through the SiO_2 potential barrier, which requires very high electric fields in the SiO_2. The high potentials on wafer surface required to produce these electric fields result from the beam ions and (primarily) from escaping secondary electrons, which produce positive potentials on the surface of a wafer when a device is under the beam. To neutralize this positive charging, electron "showers" or Plasma Flood Systems (PFS) are employed. However, the electrons from the electron "shower" or a PFS also produce negative charging when a device is outside the beam. Increasing the electron output from the electron "shower" or PFS increases the negative potentials, and decreases the positive potentials. The opposite is true when the output from the electron "shower" or PFS is reduced. Consequently, control of wafer charging in ion implanters is a matter of *balance* between positive charging, and negative charging, as illustrated in Figures 7a-7b.

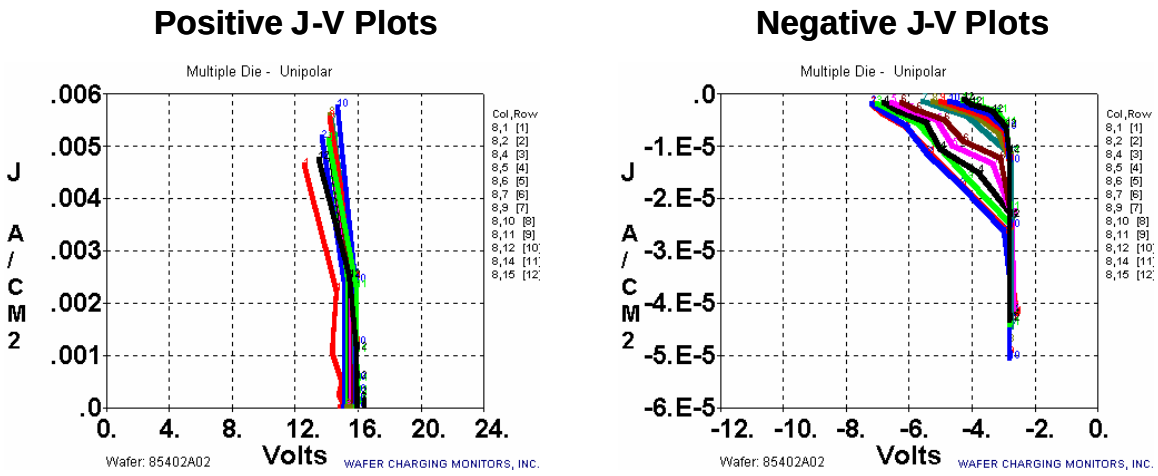


Figure 7a. High positive charging is observed during a high current implant when PFS is turned OFF.

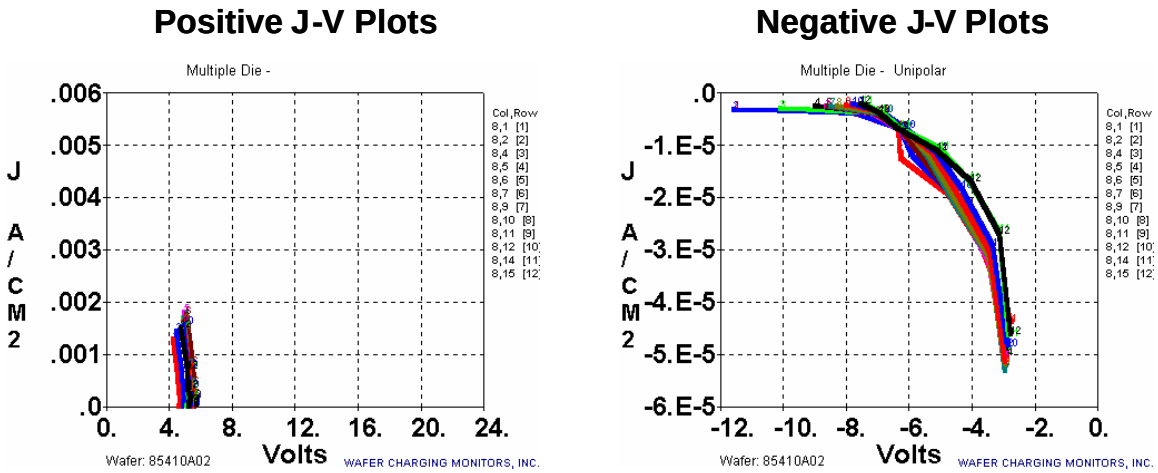


Figure 7b. Positive charging is reduced (positive J-V plots move to lower voltages) and negative charging is increased (negative J-V plots move to higher voltages) during the same implant when PFS is turned ON.

Since the high current densities encountered during positive charging [15] can be potentially very destructive, there exists a historical fear of positive charging, and a tendency to "over-flood" implants[1]. However, since charging occurs in sub-millisecond pulses, deep-depletion of the substrate, and reverse-biased wells, provide protection by absorbing a major fraction of the applied potentials. A straight-forward device analysis shows that most vulnerable are N-channel transistor during negative charging, when the full negative potentials are applied across the gate oxide [16]. Consequently, *electron showers or PFS' should be used only to bring positive charging under sufficient control so it does not overwhelm the protection provided by the transistor depletion regions and*

[1] That is, to generate more negative charge with the electron shower or PFS than is really necessary.

reverse-biased n-wells. Beyond that, negative charging should be minimized since the high negative potentials typically observed (especially in older machines) can force current into the gate oxide and cause device damage [16]. However, the subsequent high-temperature implant activation anneals can typically remove the damage *if the gate oxide is not ruptured*.

Based on the above, it also becomes apparent that charging damage in ion implanters could be eliminated if the negative potentials produced by electron "showers" or PFS' could be lowered sufficiently to avoid electron injection into the gate oxide of N-channel transistors. This could be accomplished if the electron energies were sufficiently low. Indeed, profound reduction in both positive and negative charging was observed in an ion implanter equipped with a low electron temperature (T_e) plasma flood system [17]. Implants of resist-patterned CHARM®-2 wafers showed virtual absence of "electron shading" effects, leading to the speculation that if etching tools could be implemented in a manner resembling ion implanters – where the ion and electron sources are independently adjustable – and equipped with low T_e plasma flood systems, charging damage in etching tools might be completely eliminated. This would eliminate the need for the restrictive "antenna" design rules, thereby increasing circuit density and improving circuit performance.

CHARGING MONITOR REQUIREMENTS

Since charging damage occurs as a result of potentials induced on the surface of a wafer, or a combination potentials and UV, it should be clear that a charging monitor used for the purpose of quantifying process equipment performance must be able to *separately* measure UV intensity and surface charging. Moreover, because the magnitude of gate oxide damage is proportional to the charge flux collected by "antennas" on the surface of a wafer, the monitor must also be able to quantify charge fluxes incident on the surface of a wafer. Furthermore, because charging in some tools occurs in the form of pulses – for example, transients during transitions from one operating state to another – or in the form of pulses of opposing polarity, as in ion implanters, the monitor must be able to measure the polarity of the voltage and charge fluxes of *both* positive and negative charging events to accurately quantify the charging characteristics of a process tool.

In short – it is not possible to summarize the characteristics of a process tool in a single variable, as some charging monitors attempt to do, regardless of how convenient that would be. To try to summarize charging in one or two variables grossly oversimplifies the complex nature of charging in contemporary process tools, and invariably misleads the user – often causing great expense due to delays in identifying the true source of a problem, or incorrectly assessing the effectiveness of remedial efforts.

Even damage monitors, such as the widely used "antenna" devices which attempt to directly assess the probability of damage to product wafers, may provide a misleading feeling of security when no damage is observed. This is due to the substrate antenna

effect, which can significantly change the results depending on the area of "antennas" connected to the substrate. Since this variable is typically ignored in the design of damage monitors, the results obtained by different damage monitors (or the same scribe lane monitors included on different products) are not unique, but depend on the on the area of surface "antennas" connected to the substrate.

PROPER USE OF CHARGING AND DAMAGE MONITORS

The substrate antenna effect makes some engineers uncomfortable, because it shows that results obtained with even the most widely used monitors are not absolute, but depend on the design of the monitors. But this should not cause lack of trust in the utility of the charging or damage monitors. It is a fact of nature that all measurement tools interact with the environment they try to measure[2]. The proper use of charging or damage monitors should not be, therefore, to determine if a particular level of charging is "safe", but to use the monitor to *compare* tools or processes to determine which tool or process is *better*. As long as a response is obtained on the monitor, process or tool comparisons can be done effectively even if the monitor interacts with the environment it is measuring.

CONCLUSIONS

The mechanisms by which charging damage occurs and, thus, what steps need to be taken to eliminate charging damage, were predictable years ago from the physics of charge transport in oxides [1,2]. Instead, the initial unavailability of monitors with response characteristics needed to confirm these mechanisms resulted in much confusion, and countless investigations which generated a great deal of characterization data, but, with few exceptions[3], provided little insight into the root causes of charging damage. Experiments with the CHARM®-2 charging monitors ultimately provided the missing insights and confirmed the theoretical predictions.

The conclusions are amazingly simple. *To minimize charging damage in plasma tools, plasmas must be made uniform.* This disables the UV-related damage mechanisms by eliminating the driving force for charge transport in oxides, and also minimizes the "electron shading effect". *In ion implanters, the application of moderate amounts of negative charge through the use of electron showers or plasma flood systems (PFS) is sufficient* to prevent positive charging damage, which would be destructive due to the high positive current density. Moderate application of electron "showers" or PFS' also minimizes the relatively low-level damage from negative charging. This low-level damage is then completely removed during the subsequent ion implant activation anneal.

Finally, it should be remembered that charging damage during process steps following the ion implant activation anneal are *not* annealed out by the forming gas

[2] The most fundamental statement of this effect is the well-known Heisenberg Uncertainty Principle.
[3] Most notably, the observation of the "electron shading effect".

anneal at the end of wafer fabrication. While device parameters may not appear to be affected due to the *passivating* effect of the forming gas anneal, devices remain damaged, and degrade rapidly under stess during device operation, thus affecting device reliability [18,19]. Consequently, *wafer charging during process steps following the ion implant activation anneal must be completely eliminated.*

REFERENCES

1. K. Schuegraf and C. Hu, *Semicond. Sci. Technol*., **9**, 989 (1994).
2. M. Joshi, et al, *Intl. Symp. Plasma Proc.-Induced Damage*, 23 (2002).
3. J. Suehle, and P. Chaparala, *IEEE Trans. El. Dev.*, **44**, 801 (1997)
4. G. Hwang and K. Giapis, *Intl. Symp. Plasma Proc.-Induced Damage*, 164 (1998).
5. M-Y. Lee, et al, *Intl. Symp. Plasma Proc.-Induced Damage*, 104 (1999).
6. C.K. Barlingay, et al, *Intl. Symp. Plasma Proc.-Induced Damage*, 76 (2001).
7. C.K. Barlingay, et al, *Intl. Symp. Plasma Proc.-Induced Damage*, 27 (2002).
8. E. H. Poindexter, *J. Non-Cryst. Solids* vol. **187**, 257 (1995).
9. W. L. Warren et al, *Appl. Phys. Lett*. vol. **68**, 2993 (1996).
10. K. Hashimoto, *6th Intl. MicroProcess Conf*., 114 (1993).
11. W. Lukaszek and J. Shields, *Intl. Symp. Plasma Proc.-Induced Damage*, 68 (2002).
12. W. Lukaszek, *Intl. Symp. Plasma Proc.-Induced Damage*, 26 (2000).
13. W. Lukaszek and C. Gabriel, *Intl. Symp. Plasma Proc.-Induced Damage*, 116 (2001).
14. W. Lukaszek, *Intl. Conf. Ion Implant. Tech.*, (2000)
15. W. Lukaszek, et al, *Intl. Conf. Ion Implant. Tech.*, (2002)
16. W. Lukaszek, et al, *Intl. Symp. Plasma Proc.-Induced Damage*, 200 (1999).
17. W. Lukaszek, et al, *Intl. Symp. Plasma Proc.-Induced Damage*, 182 (2003).
18. J. King and C. Hu, *IEEE El. Dev. Lett*., **15**, 475 (1974)
19. X. Y. Li, et al, *J. Vac. Sci. Technol. B*, **14**, 571 (1996)

