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Electron Shading Effects During Oxide Etching in Uniform and Non-Uniform Plasmas

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Abstract:

Potentials and current densities imposed on device structures during oxide etching due to electron shading effects are presented. Comparison of results obtained in etchers exhibiting good plasma uniformity with results from etchers exhibiting plasma non-uniformity emphasizes the importance of uniform plasma to minimize charging damage during IC manufacturing.

Introduction

Plasma charging damage to transistors due to electron shading has been widely discussed in the literature [1]. Although countless papers present damage results, only a handful of papers show direct measurements of the potentials and currents imposed on device structures in plasma tools [2,3]. This paper presents results from electron shading experiments performed with the CHARM®-2 monitors in oxide etchers exhibiting uniform and non-uniform plasmas. The results emphasize the importance of uniform plasmas to minimize charging damage during IC manufacturing.

Experimental procedures

A special-purpose six-field mask was developed to pattern resist on CHARM-2 wafers. In one field, the resist was completely removed from the entire die. In another field, the resist completely covered the entire die. In the remaining four fields, holes were patterned on the charge-collection electrodes of the potential and charge-flux sensors using 2µm, 1.5µm, 1µm, and 0.5µm design rules. The wafers were patterned using 1.2µm resist, and exposed to standard oxide etching processes in commercially available oxide etchers. An un-patterned (bare) CHARM-2 wafer was also used in each experiment to monitor plasma uniformity.

Experimental results in uniform plasma

Typical results obtained in an etcher exhibiting good plasma uniformity are illustrated in Figure 1, which shows the positive current density[1] measured in the 2µm, 1.5µm, 1µm, and 0.5µm fields. (In each pattern, the measured current was divided by the total area of the resist holes, to obtain current density in the holes in A/cm^2.)

As shown in Figure 2, J-V plots obtained with the 0.5µm pattern exhibit a tight distribution over the entire wafer, indicating good plasma uniformity. The bare control wafer confirmed this – positive and negative potentials were below the detection limit (~ 2V for this experiment), and no positive or negative currents were detected.

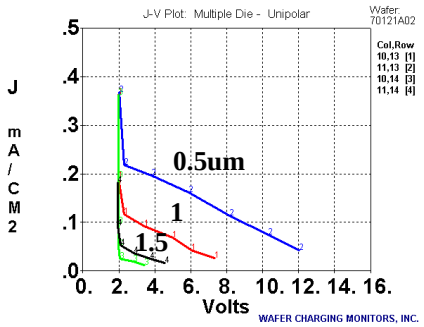

Figure 1. Positive J-V plots for 2µm, 1.5µm, 1µm, and 0.5µm holes in a uniform plasma oxide etcher. No current was recorded in the open field.

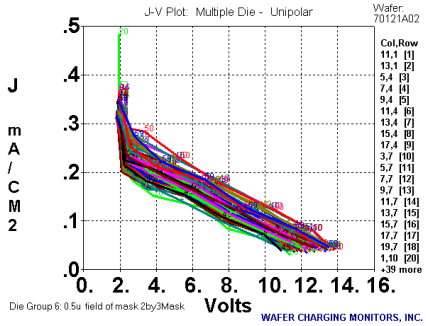

Figure 2. Distribution of positive J-V plots over the wafer for the 0.5µm pattern in a uniform plasma oxide etcher.

[1] The vertical asymptote at ~ 2V in the positive J-V graphs comes from non-responding sensors, and should be ignored.

Experimental results in non-uniform plasma

As illustrated in Figure 3, the best-case results obtained in the center of the wafer in the etcher exhibiting plasma non-uniformity are comparable to the results obtained in a uniform-plasma etcher. However, as shown in Figure 4, the worst-case results obtained at the edge of the wafer are significantly worse. (Note change of J scale in Figure 4.)

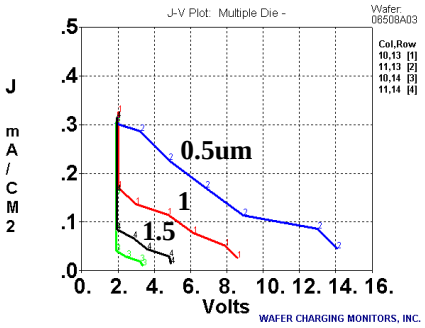

Figure 3. Best-case positive J-V plots for 2µm, 1.5µm, 1µm, and 0.5µm holes in a non-uniform plasma oxide etcher. No current was recorded in the open field.

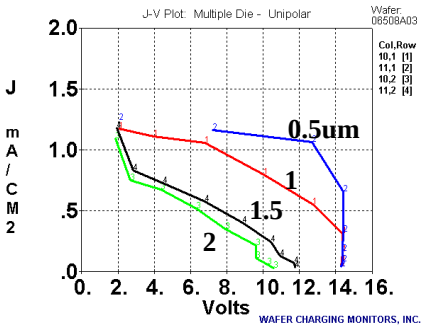

Figure 4. Worst-case positive J-V plots for 2µm, 1.5µm, 1µm, and 0.5µm holes in a non-uniform plasma oxide etcher.

The corresponding best-case and worst-case negative J-V plots[2] for the non-uniform plasma are shown in Figures 5 and 6, respectively.

The strong reduction in negative current density in the 0.5µm holes (aspect ratio of 2.4) indicates strong electron shading effects. Less intense electron shading is also evident in the 1µm holes (aspect ratio of 1.2).

[2] The vertical asymptote at ~ -2V in the negative J-V graphs comes from non-responding sensors, and should be ignored.

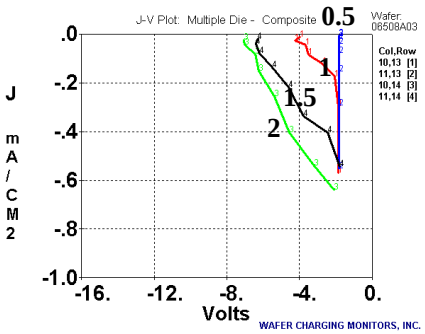

Figure 5. Best-case negative J-V plots for 2µm, 1.5µm, 1µm, and 0.5µm holes in a non-uniform plasma oxide etcher.

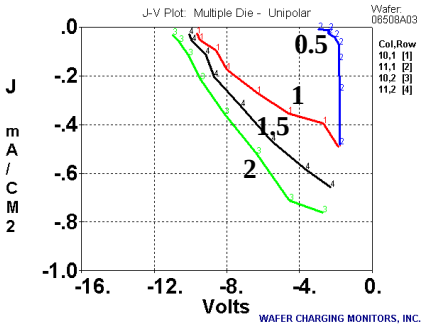

Figure 6. Worst-case negative J-V plots for 2µm, 1.5µm, 1µm, and 0.5µm holes in a non-uniform plasma oxide etcher.

The distribution of J-V plots over the wafer was also much worse than in the uniform plasma case, as illustrated in Figure 7, indicating significant plasma non-uniformity. It should be observed that the charge flux sensors are saturated at ~14V in most locations. Judged from extrapolation of the J-V plots in Figure 7 to J = 0V, positive potentials significantly higher than 14V were developed over much of the wafer.

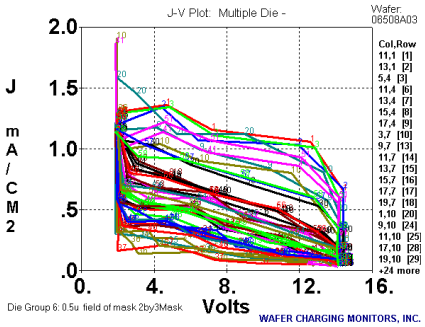

Figure 7. Distribution of positive J-V plots over the wafer for the 0.5µm pattern in a non-uniform plasma oxide etcher. (Note sensor saturation at ~14V.)

This non-uniformity was also observed with the bare control wafer. The distribution of positive and negative J-V plots on the bare wafer is shown in Figures 8 and 9, respectively.

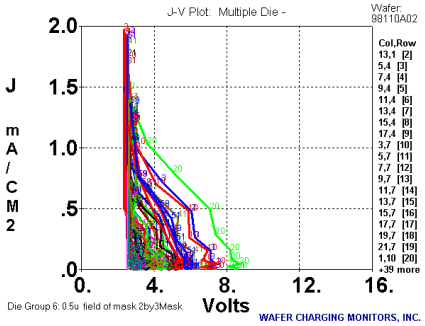

Figure 8. Distribution of positive J-V plots on a bare control wafer in a non-uniform plasma oxide etcher.

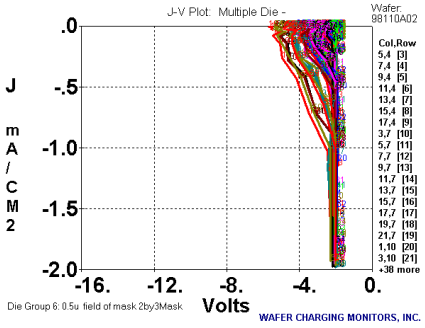

Figure 9. Distribution of negative J-V plots on a bare control wafer in a non-uniform plasma oxide etcher.

It is interesting to note that the distributions of positive and negative J-V plots recorded in the open field on the resist-patterned wafer are different from those obtained on the bare wafer. Both positive and negative J-V plots obtained on the resist-covered wafer are shifted to higher potentials, as shown in Figures 10 and 11, respectively. The shapes of the J-V plots are different, as well. This indicates that the presence of resist patterns in the other fields on the wafer influenced the results obtained in the field which had no resist in it.

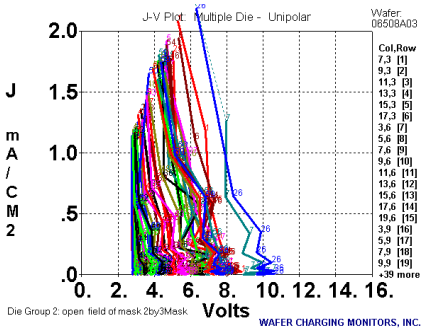

Figure 10. Distribution of positive J-V plots recorded in the open field on a resist-patterned wafer in a non-uniform plasma oxide etcher.

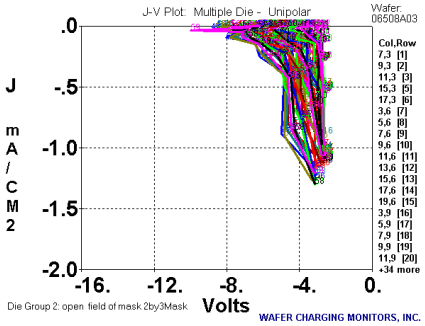

Figure 11. Distribution of negative J-V plots recorded in the open field on a resist-patterned wafer in a non-uniform plasma oxide etcher.

This behavior appears consistent with previously reported results. Enhanced positive charging was observed in a different oxide etcher on resist-covered wafers, in 100μm wide spaces opened by scribe-lanes [4]. It was also shown that both positive and negative potentials could be increased or decreased on bare wafers by decreasing or increasing the area of antennas connected to the substrate [5]. Furthermore, increased positive currents were reported in instances of low via density [6], and increased circuit damage was reported in IC regions having low via density [7].

These results could be unified under the hypothesis that reducing the amount of antenna area exposed to a plasma leads to higher surface-substrate potentials in non-uniform plasmas, independent of the presence or absence of electron shading effects. This would be consistent with a model involving electrical loading of the plasma by the wafer – the less loading, the higher the peak values.

Discussion of results

A significant increase in positive current density was observed in the 1μm and 0.5μm holes, consistent with electron shading, in both uniform and non-uniform plasmas. Even in uniform plasmas, the peak positive potentials developed in the 0.5μm holes, shown in Figures 1 and 2, are sufficient to cause conduction in contemporary gate oxides. This indicates that even uniform plasma oxide etchers are capable of causing damage in contemporary technologies, and that antenna design rules have to be employed to reduce damage to acceptable levels.

Unfortunately, this strategy is much more difficult to implement when dealing with non-uniform plasmas, which greatly increase the damaging current density. This is clearly visible in Figure 12, which shows the positive J-V plots for the 0.5μm holes at different locations from the center of the wafer, and Figure 13, which shows the positive J-V plots obtained on a bare wafer at the same die locations.

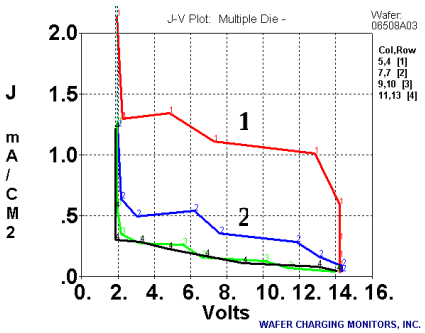

Figure 12. Positive J-V plots for 0.5µm holes at different locations from the center of the wafer. (The irregularities in the J-V plots are due to spatial charging variation within a die.)

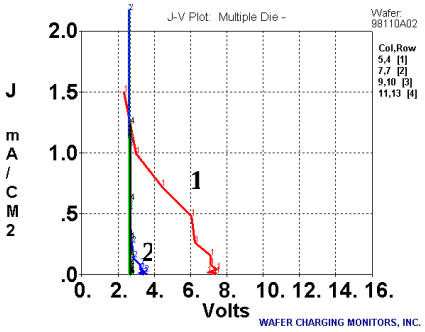

Figure 13. Positive J-V plots from a bare wafer at the same locations as shown in Figure 12. (Vertical lines at ~ 2.5V are due to non-responding sensors.)

The bottom two J-V plots in Figure 12 are due to electron shading only, since (a) they are identical, and (b) they come from a region of the wafer characterized by a uniform plasma (as evidenced by Figure 13, where the corresponding J-V plots for these locations appear as vertical lines). In the presence of plasma non-uniformity, which gives rise to J-V plots 1 and 2 in Figure 13, the corresponding J-V plots obtained with the 0.5µm holes show increased current densities. To guard against the much higher current density encountered around the periphery of the wafer (plot 1), more conservative antenna design rules would have to be employed to reduce damage to acceptable levels.

Summary and conclusions

Electron-shading characterization experiments were conducted in both uniform and non-uniform plasma oxide etchers using resist-coated CHARM-2 wafers patterned with a special-purpose electron-shading mask. Although non-uniform plasma etchers are much more likely to cause damage, the results show that even uniform-plasma etchers could cause damage to contemporary gate oxides.

Since the electron-shading effect and plasma non-uniformity are independent effects, their contributions are additive. Consequently, much higher charging currents are developed during oxide etching in regions of plasma non-uniformity, requiring more conservative antenna design rules to limit damage to acceptable levels. Conversely, to minimize damage during wafer manufacturing (when the design cannot be changed), plasma non-uniformity needs to be eliminated.

More evidence was also presented indicating that an additional mechanism exists in non-uniform plasma, which increases *both* positive and negative potentials under conditions which (along with possibly other, yet to be identified variables) restrict current paths through the wafer. A hypothesis regarding the possible nature of this mechanism was proposed.

Acknowledgments

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