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Quantifying Via Charging Currents

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Abstract

Via charging currents during via over-etch have been measured for the first time using CHARM®-2 wafers and a special-purpose CHARM®-2-compatible photoresist mask with varying via density. The measurements confirm previous findings which showed increased charging potentials and current densities in the presence of patterned resist [1]. The measurements also show the presence of an additional effect - an increase in via charging currents with decreasing via density. This effect may have considerable implications for product damage, and for the evaluation and analysis of resist aspect-ratio dependent charging damage.

I. Introduction

Plasma processing-induced charging damage through contacts and vias has typically been studied using antenna capacitors **[2]**, which employ thin gate oxides to sense and record the damage. However, since the extent of damage depends on oxide thickness and quality, the results are not a universal measure of equipment performance. The calibrated CHARM®-2 wafers **[3]**, populated with electrostatic potential, current-density, and UV sensors, provide universally comparable results, since the wafer surface-substrate potentials are measured in volts, and the J-V characteristics of the charging source are measured in amps/cm2.

Previous characterization **[1]** of wafer charging in a LAM 384T triode etcher using CHARM®-2 wafers led to the observation that both voltages and current densities increased substantially (relative to results obtained with bare wafers) when a photoresist pattern was placed on the CHARM®-2 wafer. However, since the resist was patterned using a product via mask, which did not align to the charge-collection-electrodes (CCEs) of the CHARM®-2 wafer, it was not possible to quantify precisely the charging current densities.

In this paper, we describe measurements of via charging currents in the LAM 384T triode etcher using photoresist patterned with a mask specifically designed to align to the CHARM®-2 wafer. For the first time, accurate measurement of via current densities were obtained. Moreover, enhanced charging at low via density was observed, which has implications for product damage, and emphasizes the importance of pattern density considerations in the evaluation of resist aspect-ratio-dependent charging.

II. Motivation

Although countless investigations of charging damage to “antenna” capacitors have been carried out to establish the charging performance of various IC plasma processing equipment, the results cannot be used to predict charging damage to gate oxides of different thickness than those used in the “antenna” capacitors during the particular experiments.

In order to predict charging damage to gate oxides whose Fowler-Nordheim characteristics are known, and whose charge-to-breakdown, Qbd, has been characterized, it is essential to know the plasma charging current. From it, the charge absorbed by the oxide could be computed as $Qox = Ar\ (Jox)(t)$, where t is the charging time, Ar is the “antenna ratio” of the capacitor, and Jox is the plasma net current density on the surface of the wafer at the oxide conduction voltage, obtained from the J-V characteristics of the plasma source.

The CHARM®-2 technique [3], briefly described in [4], may be used to measure the J-V characteristics of the charging source as seen by devices on the surface of the wafer, and was chosen to quantify the via charging current J-V characteristics as a prelude to device damage prediction experiments. To this end, a special-purpose, CHARM®-2 compatible

resist mask was designed. Since previous work suggested that restricting the current collection area on the surface of the wafer by the presence of patterned resist elevated the surface-substrate potentials and current densities in the open areas (resist aspect ratio was ruled out as a possible cause due to the very large geometries **[1]**), a four-field mask was developed to explore the impact of pattern density on the via charging currents. Each field contained different density of via holes, and aligned to a separate die on the CHARM®-2 wafer.

III. The experiment

Two CHARM®-2 wafers were used in the experiment. One of the wafers was bare, the other wafer was patterned with the special-purpose resist mask. Photoresist covered the entire wafer area, except for the via holes which aligned to the CCEs of the potential and charge-flux sensors.

The density of the 1.5um x1.5 um via holes in each field was as follows:

Field name	No. of vias/CCE	Via density (1 via/um2)
v64	7936	1/25
v16	1984	1/100
v4	496	1/400
v1	124	1/1600

Both wafers were exposed to an abbreviated via etch step in the LAM 384T triode etcher.

IV. Experimental results

As in the previous experiment **[1]**, the bare wafer recorded elevated positive potentials in the center of the wafer, as shown in the wafer map of **Figure 1**, indicating a plasma non-uniformity. (The potential sensors are saturated in the center of the wafer - actual values may be greater.)

As in the previous experiment **[1]**, the wafer covered with photoresist recorded elevated potentials over a much greater portion of the wafer, as shown in the wafer map of **Figure 2.** (The potential sensors are saturated over most of the wafer.)

The corresponding relative responses of the charge-flux sensors in each of the four fields are shown in the I-V characteristics of **Figure 3.** (Since the voltage sensors saturated at 15-16 V, the voltage response of the charge-flux-sensors also saturates at 15-16 V.)

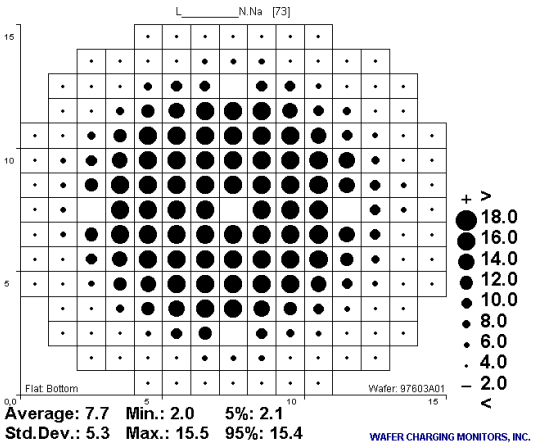

Figure 1. Positive potentials recorded by a bare CHARM®-2 wafer during abbreviated via etch (potential sensors are saturated in the center of the wafer).

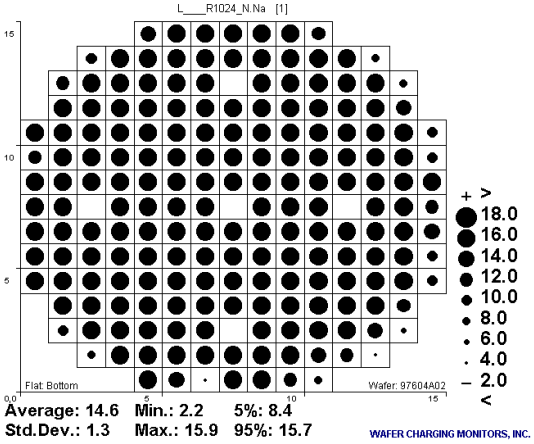

Figure 2. Positive potentials recorded by a resist-covered CHARM®-2 wafer during abbreviated via etch (potential sensors are saturated over most of the wafer).

As can be seen from **Figure 3**, the current scales with the number of vias for fields v64, v16, and v4, but not for field v1. This is apparent more clearly in **Figure 4**, which shows the results of **Figure 3**, normalized by the total area of the via openings incident on the CCEs in the respective fields, to show the via current density. As can be seen from **Figure 4,** the via current density remains constant for the three most dense patterns, but increases for the least dense pattern.

These results are reproducible, as shown in **Figures 5 and 6**, which show the J-V characteristics of the

current collected by the vias in field v1 and field v4, respectively, for several locations on the wafer. (The results for field v16 and v64 are identical to those obtained for field v4.)

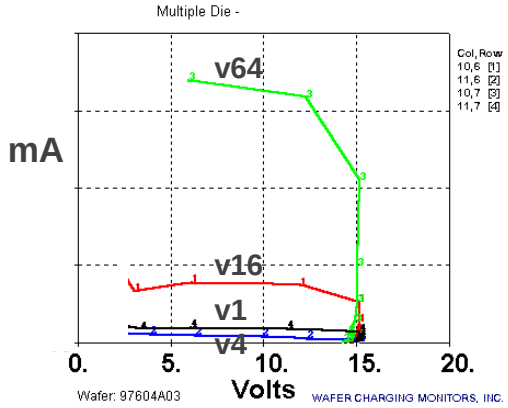

Figure 3. Relative I-V plots recorded by charge-flux sensors in each of the four fields. (The voltage response of the charge-flux-sensors saturated at 15-16 V.)

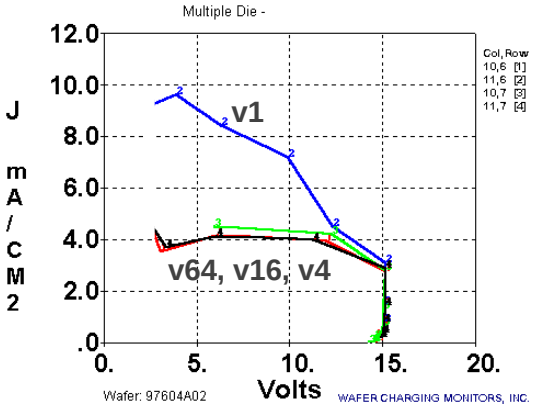

Figure 4. Via current density vs. voltage in each of the four fields. (The voltage response of the charge-flux-sensors saturated at 15-16 V.)

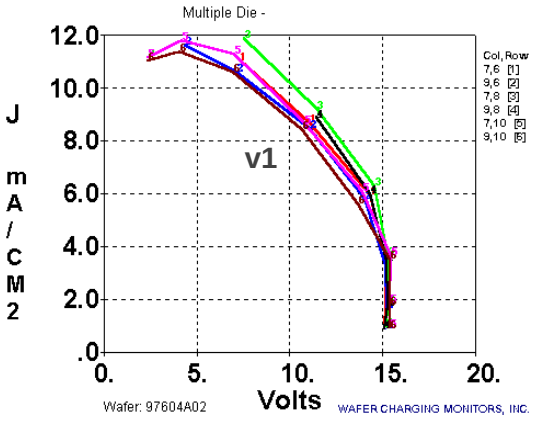

Figure 5. Via current density vs. voltage for several locations of field v1. (The voltage response of the charge-flux-sensors saturated at 15-16 V.)

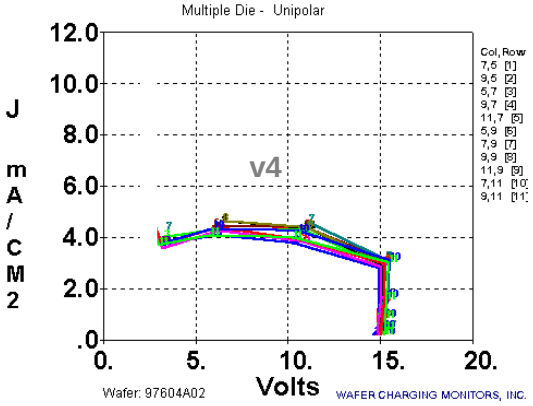

Figure 6. Via current density vs. voltage for several locations of field v4. (The voltage response of the charge-flux-sensors saturated at 15-16 V.)

V. Discussion of results

The observed dependence of charging current density on via density has several troublesome implications. For this particular equipment, it means that not all products manufactured with this process experience the same charging effects. Products, or sections of a product, having via density similar to or lower than field v1 could experience greater damage than products, or sections of a product, having higher via density. This would be consistent with results reported by Miyamoto, et. al. **[5].**

From the viewpoint of quantitative modeling of charging damage, these results imply that techniques used for measuring charging currents need to take pattern density into account, or at least verify if its influence is present or absent. The same

considerations apply to similar charging studies using “antenna” capacitors.

Finally, given the impact of resist aspect-ratio dependent charging on equipment design **[6]**, studies exploring the dependence of charging on photoresist aspect ratio should include controls to verify if the equipment being evaluated exhibits the charging behavior described in this paper. If the results indicate similar behavior, additional controls should be employed to ensure that results attributed to higher aspect ratio are not due to global reduction in charge collection area when the dimensions of the patterned elements are reduced.

VI. Summary

For the first time, current density collected by vias during the over-etch portion of via etching was measured using CHARM®-2 wafers and a four-field photoresist mask with variable pattern density. It was observed that the current density remained constant over a wide range of via density. However, at low via density, the charging current increased substantially. Unfortunately, via density similar to that used in the least dense pattern is common in many products.

These results also underscore the importance of pattern density considerations in the design of test vehicles and resist masks used for the evaluation of resist aspect-ratio-dependent charging.

VII. References

[1] W. Lukaszek and A. Birrell, “Quantifying Wafer Charging During Via Etch”, 1996 1st International Symposium on Plasma Process-Induced Damage, Santa Clara, CA, May 13-14, pp. 30-33.

[2] C. Gabriel, et. al. , “Plasma Processing-Induced Charging Through Contacts and Vias”, 1995 VLSI Multilevel Interconnection Conference, June 27-29, 1995, pp. 394-396.

[3] W. Lukaszek, "The Fundamentals of CHARM®-2", Technical Note 1, Wafer Charging Monitors, Inc., 127 Marine Road, Woodside, CA, 94062.

[4] W. Lukaszek, “Characterization of Wafer Charging in ECR Etching”, these proceedings.

[5] K. Miyamoto, et. al., “Impact of Pattern Density on Plasma Damage of CMOS LSIs”, 1996 IEDM, pp. 739-742.

[6] K. Hashimoto, et. al., “Reduction of the charging damage from electron shading”, 1996 1st International Symposium on Plasma Process-Induced Damage, Santa Clara, CA, May 13-14, pp. 43-46.