Characterization of Wafer Charging in ECR Etching

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Abstract

A CHARM®-2 investigation of wafer charging during ECR etching revealed regions of highly localized negative charging, with current densities approaching -3 mA/cm2 at -10 V. The highly localized regions of negative charging emphasize the need for ECR etcher characterization using charging monitors having high spatial resolution, and means for verifying the certainty of results.

I. Introduction

The continued scaling of MOS transistor gate oxides in contemporary IC technologies places increasingly stringent requirements on the charging performance of plasma etching equipment. Typical chargingdamage characterization of such equipment is carried out with "antenna" capacitors [1] which employ gate oxides as the sensing elements. Due to the inevitable variation in the microscopic structural properties of the gate oxide, the results are statistical in nature. This lack of precision may be acceptable if the equipment charging characteristics vary gradually over the wafer, causing sufficient number of adjacent failures to accurately map the region of high charging damage. However, the interpretation of isolated failures becomes more difficult: Should they be attributed to local variation in oxide quality, or to the charging characteristics of the equipment? This question becomes particularly vexing in the case of magnetically-enhanced plasma sources, where improper management of magnetic fields may cause highly localized charging.

In this paper we present results obtained with the CHARM®-2 charging monitor which show that highly localized charging is observed in ECR etchers, and that it is possible to determine the presence of this localized charging with high degree of certainty using the CHARM®-2 charging monitors.

II. Description of CHARM®-2

In order to make the following results more meaningful, it is important to understand the capabilities of the CHARM®-2 technique. The CHARM®-2 wafers are composed of 8mm x 8mm die populated with EEPROM-based, *calibrated*,

polarity-sensitive sensors of wafer surface-substrate potentials, net charge flux, and UV dose [2,3].

The CHARM®-2 potential sensors are implemented by connecting a charge collection electrode (CCE) on the surface of the wafer to the control-gate of an EEPROM transistor, as shown in **Figure 1**. The CHARM®-2 potential sensors thus resemble the widely used "antenna" devices, except that in CHARM®-2 the sensing element is not gate oxide, but an EEPROM transistor, whose threshold voltage is changed by the voltage developed on the CCE. The potential sensors used in this study were spaced vertically, 960 um apart.

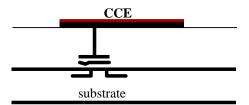


Figure 1. CHARM®-2 potential sensor.

The CHARM®-2 charge-flux sensors are implemented by adding current-sensing resistors between the CCE and the substrate of the potential sensors, as shown **Figure 2**. In this configuration, the EEPROM transistor is used to measure the voltage across the current-sensing resistor, from which the current density may be determined.

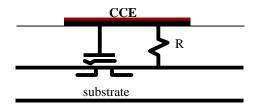


Figure 2. CHARM®-2 charge-flux sensor.

The CHARM®-2 wafers implement twelve chargeflux sensors to span a range of four and a half orders of magnitude in current densities. The closely ratioed current-sensing resistors permit reconstruction of the J-V characteristics of the charging source from the charge-flux sensor data, as shown in Figure 3. (In the J-V plane, each resistor is represented by a straight line with a slope of 1/R. Since the response of each sensor must lie on that line, each sensor provides one point in the J-V plane, and the collection of (J,V) values obtained from the set of CHARM®-2 current sensors allows reconstruction of the J-V characteristics of the charging source.) The set of CHARM®-2 chargeflux sensors thus implements a passive plasma probe to quantify, on the wafer surface, that portion of the plasma J-V characteristic where the plasma delivers power to the wafer, which is responsible for device damage.

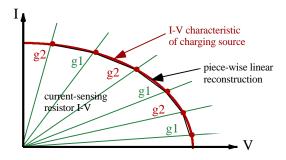


Figure 3. Charge-flux sensors with different value current sensing resistors allow re-construction of the J-V characteristics of the charging source (g1 =sensor in group 1; g2 =sensor in group 2; the two groups are spaced 4 mm apart).

The charge-flux sensors used in this study are located in two groups, spaced horizontally 4 mm apart. Each of the two groups contain six sensors, and the values of the current-sensing resistors alternate between the two groups as shown in **Figure 3**. As a result of this, spatially uniform charging gives rise to smooth J-V plots, whereas spatially varying charging gives rise to J-V plots showing pronounced "zig-zag", indicating that the two groups of sensors experience different charging environments which should be represented with two distinct J-V plots, one for each group of sensors.

III. Experimental results

A calibrated CHARM®-2 wafer was exposed to an etch process in an ECR etcher. The peak potentials recorded by one of the positive potential sensors, the

GR_S_10.Na, are shown in **Figure 4.** Both sensors recorded virtually identical results, with gradual variation of positive potential over the wafer.

The positive J-V plots for six die on a vertical line from the center of the wafer to the edge of the wafer, shown in **Figure 5**, also show smooth behavior, indicating that the spatial variation in charging within the 4 mm distance between the two groups of charge flux sensors is small. All of this implies that positive charging varied relatively slowly over the wafer.

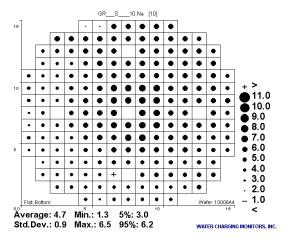


Figure 4. Peak positive potentials recorded by the GR_S_10.Na potential sensors.

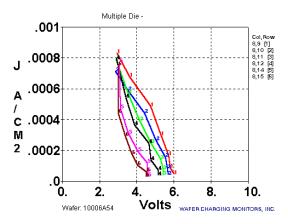


Figure 5. Positive J-V characteristics (1 = center of the wafer, 6 = edge of the wafer).

On the other hand, the peak potentials recorded by the GR_S_10.Pa and GR_S_30.Pa negative potential sensors, shown in **Figures 6 and 7**, show rapid spatial variation at several locations on the wafer. Moreover, even though the pattern appears similar in both cases, close examination of the affected areas reveals substantial variation in the values recorded

by the two sensors, as shown in **Figure 8** for one such area, even though the sensors are spaced less than 1 mm apart.

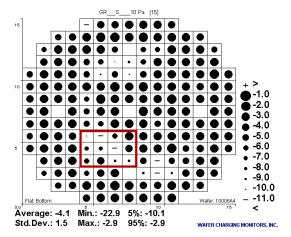


Figure 6. Peak negative potentials recorded by the GR_S_10.Pa potential sensors. Values in the selected area are shown in **Figure 8**.

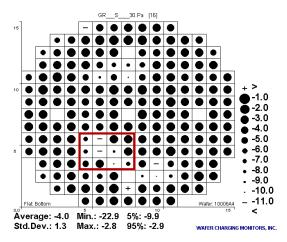


Figure 7. Peak negative potentials recorded by the GR_S_30.Pa potential sensors. Values in the selected area are shown in **Figure 8**.

-10.	-14.	-6.5	-3.1	-7.3	-11.	-3.6	-3.1
-7.9	-7.1	-13.	-4 .6	-7.4	-12.	-9.6	-3.1
-6.6	-4. 4	-9.1	-9.6	-5.1	-3.9	-11.	-7.4

Figure 8. Peak negative potentials recorded by the GR_S_10.Pa and GR_S_30.Pa sensors are different in a region affected by rapid spatial variation in negative potentials (the sensors are less than 1 mm apart).

Analogous results are obtained with the charge-flux sensors, as illustrated in **Figure 9**, which shows the negative J-V characteristics of three die in the area selected in **Figure 8**. The smooth behavior of plot 2 indicates relatively uniform charging in die (col. 7, row 5). This, and the very large current density suggest that die (7,5) was situated at the local peak of negative charging. The die on either side of die (7,5) experienced considerably lower current densities, as evidenced by plot 1 (corresponding to die (6,5)), and plot 3 (corresponding to die (8,5)).

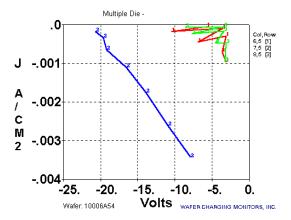


Figure 9. Negative J-V plots for three die in region of rapid spatial variation in negative charging (columns 6, 7, 8; row 5).

Plots 1 and 3 also exhibit the "zig-zag" pattern characteristic of a rapidly spatially varying charging environment, where one group of sensors experiences a different charging intensity than the other. It should be noted that plot 1 shows a "zig-zag" pattern which is opposite to the pattern of plot 3. The expanded version of plot 1, shown in **Figure 10**, indicates that the sensors in group 2 recorded a much stronger response than sensors in group 1. In the expanded version of plot 3, shown in **Figure 11**, the opposite is observed.

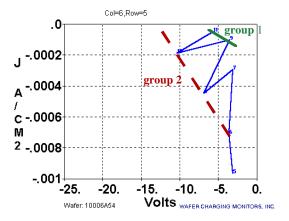


Figure 10. Expanded scale negative J-V plot for die in column 6, row 5.

The results recorded in die (6,5), (7,5), and (8,5), and shown in **Figure 9**, thus suggest the spatial distribution of negative charging depicted in **Figure 12**. Since the center of charging is located over the upper portion of die (7,5), die (6,5) experiences more intense charging over the second group of sensors (g2), while die (8,5) experiences more intense charging over the first group of sensors (g1), in accordance with **Figures 10** and **11**.

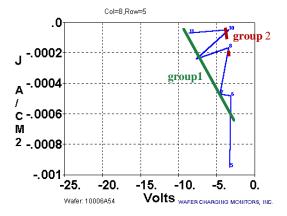


Figure 11. Expanded scale negative J-V plot for die in column 8, row 5.

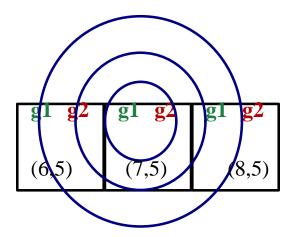


Figure 12. Approximate location of the negative charging summarized in **Figure 9:** (6,5), (7,5) and (8,5) are the die locations of J-V plots in **Figure 9**; g1 and g2 represent the approximate location of the two groups of charge-flux sensors.

IV. Summary

Although the nearly perfect mirror-symmetry of the negative J-V plots shown in **Figure 9** was not always

observed, the complementary "zig-zag" behavior of the negative J-V plots was observed in virtually all adjacent die affected by negative charging shown in **Figures 6 and 7**. This confirms the presence of multiple, highly localized peaks of negative charging. As indicated by the data in **Figure 8**, large variations in negative charging are observed by devices less than 1 mm apart.

Given these observations, charging evaluation of ECR plasma sources should be done with monitors having high spatial resolution, and the ability to confirm that the results are not due to local artifacts associated with the monitor. Due to its fundamental approach, and its comprehensive set of sensors, CHARM®-2 is a good candidate for this task.

V. References

[1] C. Gabriel and J. McVittie, "How Plasma Etching Damages Thin Gate Oxides", Solid State Technology, June 1992, pp. 81-87.

[2] W. Lukaszek, "The Fundamentals of CHARM®-2", Technical Note 1, Wafer Charging Monitors, Inc., 127 Marine Road, Woodside, CA, 94062.

[3] W. Lukaszek and A. Birrell, "Quantifying Wafer Charging During Via Etch", 1996 1st International Symposium on Plasma Process-Induced Damage, Santa Clara, CA, May 13-14, pp. 30-33.

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