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Photoresist Mask Design for Evaluation of Resist-Mediated Charging Effects During High Current Ion Implantation

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Abstract - Although the effects of photoresist on wafer charging during high current ion implantation have been previously reported [1-4], the resist layouts did not always simulate resist placement on product wafers, making it difficult to determine how relevant the results were to charging experienced by product wafers. Building on previous work, this presentation describes a general approach to resist mask design, intended to emulate resist placement on product wafers. This approach is applied to the design of four-field reticles for use with the CHARM®-2 monitors to provide a tool for optimization of implant conditions to minimize resist-mediated charging on product wafers, and to provide a basis for empirically-based modeling of resist-mediated charging phenomena. Both dark-field and light-field designs are described. The masks described here were used in a comprehensive study of resist-mediated wafer charging on the Applied Materials 9500xR [5].

I. Introduction

The important influence of photoresist on wafer charging during ion implantation has been recognized for quite some time, and has been the subject of numerous papers attempting to provide an understanding of the mechanisms involved **[1-4].** From a practical point of view, the utility of past work is limited due to (a) resist layouts which did not reflect resist layuot on product wafers or were limited in scope, and/or (b) the use of damage test structures to record the extent of wafer charging. Since damage test structures, such as "antenna" capacitors, provide no information regarding the polarities and magnitudes of the charging potentials and currents, it is very difficult to correctly infer from them the details of the physical mechanisms responsible for device charging damage.

In this work, we attempted to overcome these limitations by using CHARM-2 wafers **[6]** as the charging monitors, and employing resist layouts emulating resist placement on product wafers. The primary objective of the work was to develop a practical tool to provide feedback for optimization of machine designs and implant parameters affecting resist-mediated wafer charging for all resist layout configurations. In addition, it was desired to develop a tool for the measurement of parameters, e.g. potentials and current densities, which could be used to model charging of arbitrary combinations of device and resist layouts.

II. Resist mask layout

The layout of implant resist masks for product wafers is very complex, since it must satisfy the requirements of devices made at every location on the wafer. However, all layouts must satisfy two requirements: they must allow implantation of some devices, while shielding the complementary devices. In both cases, two additional situations are encountered. If the device is being implanted, the device gate electrode is either completely within the resist opening, or, as is the case in CMOS, some portion of the gate electrode is within the resist opening but the remainder is covered by the resist. Conversely, if the device is not being implanted, the device gate electrode is either completely covered by the resist, or a portion of the gate electrode is covered by the resist while the remainder is not covered by resist. These four distinct combinations of gate/resist placements, are arranged in four separate resist fields aligned to four separate die on the CHARM-2 wafers. The CHARM-2 charge collection electrodes (CCEs) emulate the transistor gates on product wafers, allowing the measurement of polarity and magnitude of gate-to-substrate potentials, and the polarity and magnitude of charge fluxes collected by transistor gates.

This arrangement of resist layout in each field, in relation to the CHARM-2 CCEs, for dark-field masks (i. e. masks where most of the area is covered by resist, except for "holes" which comprise a small portion of the total die area) is shown in Fig. 1a, 1b, 1c, and 1d. The resist layout which emulates the case where the gate electrodes are completely exposed to the ion implant is shown in Fig. 1a. The resist is always outside the CCE and the E^2PROM transistor probe pad (the "OUT" layout). The case that occurs in CMOS, where a portion of the gate electrode is within the resist opening but the remainder is covered by resist, is emulated in the layout shown in Fig. 1b. In this case, the resist edge is inside the CCE and the E^2PROM transistor probe pad (the "IN" layout).

The complementary cases for transistors shielded from the implant by the resist are shown in Fig. 1c, and Fig. 1d.

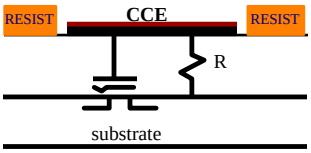

Fig. 1a. OUT layout

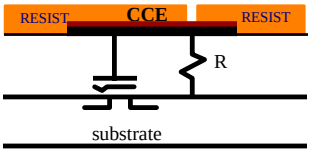

Fig. 1c. COV layout

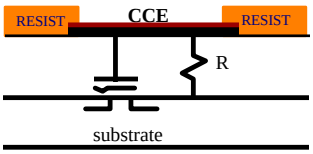

Fig. 1b. IN layout

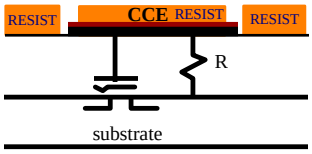

Fig. 1d. EDGE layout

The "COV" layout was intended to emulate the case where the transistor gates are completely covered with resist. This would have required that the CCE and the E^2PROM transistor probe pad be completely covered with resist. However, this arrangement would not have permitted probing of the CHARM-2 wafer without removing the resist. In turn, this would not have allowed us to "re-use" previously implanted resist in follow-on implants intended to study the evolution of charging as a function of implant dose [5]. This requirement forced a compromise layout, where the CCE is covered by the resist, while the E^2PROM transistor probe pad is not covered by resist. This is indicated in Fig. 1c by a small opening in the resist covering the CCE. Consequently, this layout actually represents a case similar to the "IN" layout, but the implanted CCE area is about 20X smaller. As such, the "IN" and "COV" layuots represent the extremes of the most interesting occurrence in CMOS processing, where a portion of the transistor gate is exposed to the implant, while the rest is covered by resist: the "IN" layout represents the case where most of the transistor gate is exposed to the implant, while the "COV" layuot represents the case where most of the transistor gate is covered by the resist. The pure case of resist completely covering the transistor gate is not represented in these layouts. What happens in this case, however, may be emulated by using a wafer half-covered with resist, as was done in a previous experiment [2].

The "EDGE" layout shown in Fig. 1d represents the case where most of the transistor gate is covered by the resist while a small portion of the gate is exposed to the implant, and the resist covering the gate is disconnected from the resist covering the field.

In all of these cases the resist-edge to CCE-edge spacing was set at 3 um.

Since the CHARM-2 wafers contain both area and edge-intensive CCEs, the same layouts were implemented on both area and edge-intensive CCEs. The "fingers" in edge-intensive CCEs are 10 um wide. Consequently, the openings in the resist on the edge-intensive CCEs in the "IN" layout are 4 um wide, compared to 94 um on the area CCEs. In future work, the edge-intensive CCEs will be used to examine the effect of narrower resist openings.

To examine the difference in resist-mediated charging between dark-field and light-field masks intended to accomplish the same task, a light-field design was also implemented. (In a light-field mask most of the area is not covered by resist, except for small "islands" of resist which comprise a small portion of the total die area.) In the light-field mask, three separate fields were implemented. The "COV" field, intended to emulate the case where the transistor gates are completely covered by resist, is the complement of the "OUT" field in the dark-field design. In order to "re-use" previously implanted resist in follow-on implants intended to study the evolution of charging as a function of implant dose, the E^2PROM transistor probe pad is not covered by resist. The "IN" field, intended to emulate the case where the transistor gates are partly covered by resist and partly exposed to the implant, is the complement of the "IN" field in the dark-field design. The E^2PROM transistor probe pad is also not covered by resist. The "EDGE" field in the light-field design is the complement of the "EDGE" field in the dark-field design. These three fields thus emulate the CMOS case where a portion of the transistor gate is covered by resist and a portion is exposed to the implant, but the three fields differ significantly in the fraction of the CCE that is covered by resist vs. being exposed to the implant.

III. Basis for modeli ng of resist-mediated charging

As shown in the following section, significant differences were observed in the charging potentials and current densities depending on the resist layout [5], and mask polarity. From a practical point of view, it is desirable to simulate the effects involved, to be able to predict charging damage to device gate oxides as function of device and resist layouts. The large differences in area-to-edge ratios of the resist layouts used in these resist masks are intended to promote separation of the measured charging currents into area- and edge-related components, thereby providing a basis for empirically-based modeling of device charging during ion implantation. Once the edge and area-related components of charging currents are quantified, the damage to device structures may be predicted from gate oxide Fowler-Nordheim characteristics, charge-to-damage relationships [6], and device and resist layout parameters. At the very least, analysis of the measured current densities as function of the features of the resist layouts can corroborate or disprove the existence of mechanisms proposed on the basis of device damage studies [1,4].

IV. Results

An extensive matrix of Arsenic implants [5] done in the Applied Materials 9500xR implanter at energies of 40, 60, and 120 KeV and dose ranging from 1e14 to 1e16 revealed large differences in the charging potentials and current

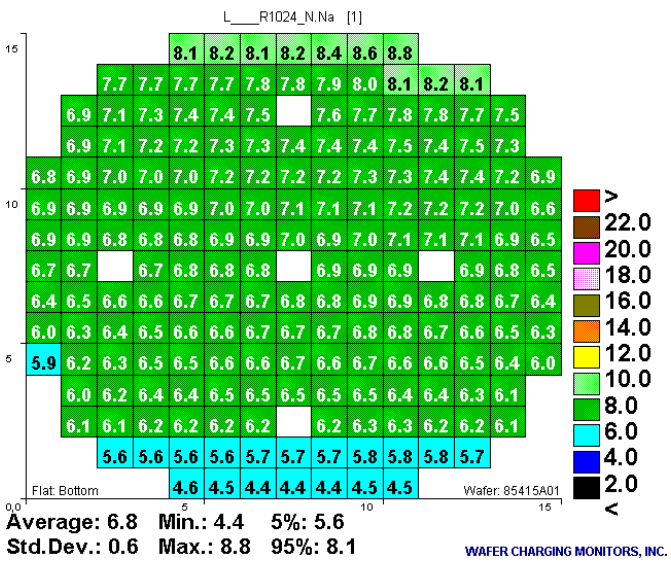

Fig. 2a. Positive potentials recorded by a bare CHARM-2 wafer during 40 KeV, 2e15, Arsenic implant.

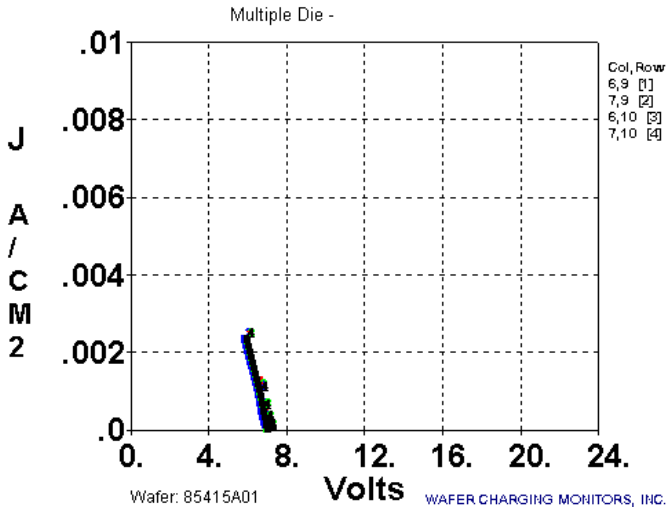

Fig. 2b. Positive J-V plots recorded by a bare CHARM-2 wafer during 40 KeV, 2e15, Arsenic implant.

densities recorded with the CHARM-2 sensors depending on the resist layout, dose, energy, and mask polarity. Some of the data obtained from this experiment is discussed below.

Fig. 2a shows the positive potentials recorded on a bare (i. e., not covered with resist) 150mm CHARM-2 wafer during a 40 KeV, 2e15, Arsenic implant under nominal implant conditions. The corresponding positive J-V plots for four die near the center of the wafer are shown in Fig. 2b. (The positive J-V plots represent the net positive current density collected on the surface of the wafer, as function of the wafer surface-substrate potential. The CHARM-2 wafers used in this experiment were optimized for low-current sensitivity.

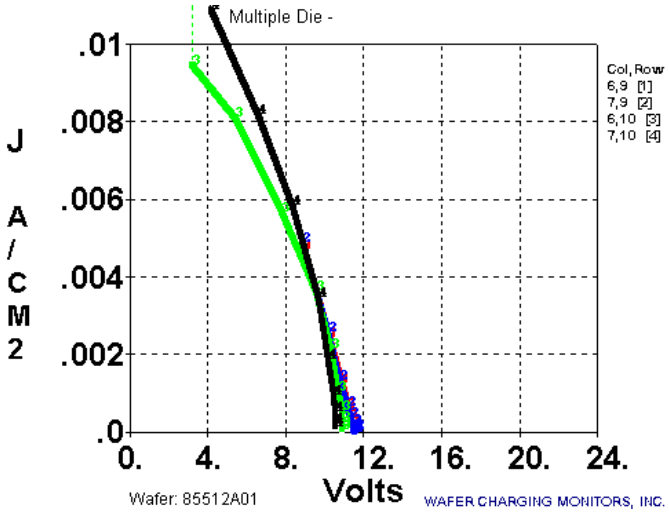

Fig. 3. Positive J-V plots recorded by a resist-covered CHARM-2 wafer during 40 KeV, 2e15, Arsenic implant. The resist was patterned with a four-field, **dark**-field mask. Plot 4 corresponds to the COV field, and plot 3 corresponds to the EDGE field described in Figure1. Plot 1 corresponds to the OUT field, while plot 2 corresponds to the IN field. Plots 1 and 2 coincide with plots 3 and 4.

Consequently, the dynamic range for large current densities is limited.)

For comparison, Fig. 3 shows the positive J-V plots for the same implant, on the same die as shown in Fig. 2b, for the case a CHARM-2 wafer covered with resist patterned with the four-field dark-field mask described in Section II. (In computing the "J" values, the measured current was divided by the area of the resist opening.) First of all, Fig. 3 shows that the presence of the resist patterns shifted the positive J-V plots to higher positive potentials (~ 11V vs. ~7V for the bare wafer). Depending on product gate oxide thickness, this change could result in a significant increase in device damage. Second, the highest current densities were obtained on the "COV" field (plot 4), where the resist covers the CCE, except for the probe pad. However, given the large differences in the exposed areas (a factor of 20X), it is remarkable that the J-V plots from the four different fields are essentially the same. >From a modeling point of view, this indicates that positive charging currents for any resist layout (for 40 KeV Arsenic implants) may be obtained by simply multiplying the measured positive current density by the exposed area, i. e. periphery-related positive currents are not significant. However, this is not the case for 120 KeV Arsenic implants, as described in [5], where large differences in positive potentials and current densities were obtained in the four different fields.

For the case of a light-field mask, the positive J-V plots obtained for a 40 KeV Arsenic implant in the three different fields (one field was repeated twice) also coincide, as shown in Fig. 4. However, the peak positive potentials (V at J = 0) are similar to those obtained with a bare wafer.

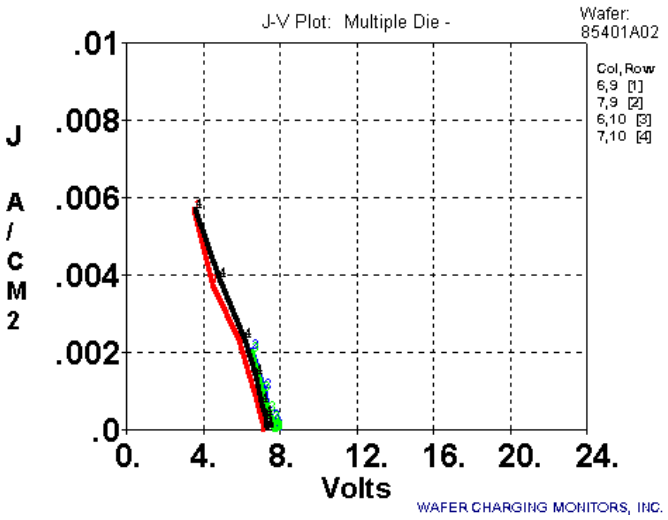

Fig. 4. Positive J-V plots recorded by a resist-covered CHARM-2 wafer during 40 KeV, 2e15, Arsenic implant. The resist was patterned with a four-field, **light**-field mask. The four plots from the three different fields coincide. The peak potentials are similar to those obtained with a bare wafer, shown in Fig. 2a.

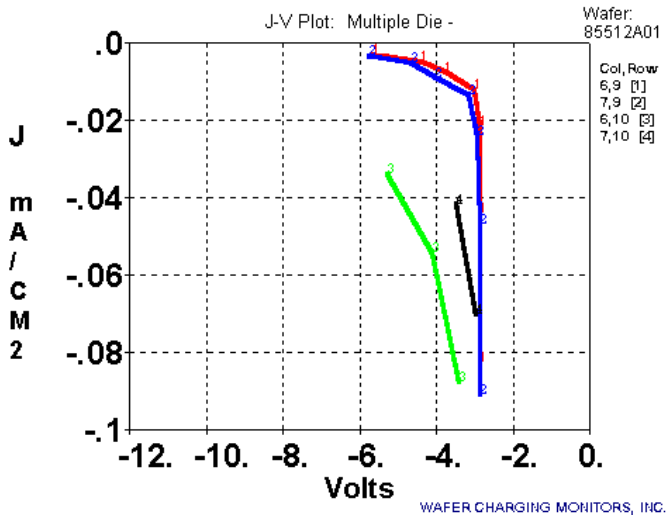

Fig. 5. Negative J-V plots recorded by a resist-covered CHARM-2 wafer during 40 KeV, 2e15, Arsenic implant. The resist was patterned with a four-field, **dark**-field mask. Plot 4 corresponds to the COV field, plot 3 corresponds to the EDGE field, plot 1 corresponds to the OUT field, and plot 2 corresponds to the IN field.

This result indicates that light-field masks should be preferred for ion implants over dark-field masks, since they do not elevate positive potentials (associated with large current densities). Suppressing increased positive potentials with electron flood results in higher negative current densities for devices not under the beam. Since the negative current densities exhibit a long "tail" which can reach relatively high negative potentials, excessive electron flood can promote charging damage due to negative charging.

The difference in charging potentials between the dark-field and light-field masks obtained in this experiment also indicates that, depending on the polarity of the implant mask, different electron flood settings should be used for optimum charging performance.

In contrast to the results obtained for positive charging, negative current densities do not exhibit the same behavior. Fig. 5 shows the negative J-V plots obtained for the 40 KeV, 2e15, Arsenic implants in the same four fields of the dark-field mask used to obtain the positive J-V plots of Fig. 3. Although the results from the IN and OUT fields, are quite similar, the results from the fields emulating the case of gates mostly covered by resist are considerably different.

IV. Summary

An approach to resist mask layout for the purpose of providing feedback for optimization of machine designs and implant parameters affecting resist-mediated wafer charging has been presented. The approach uses CHARM-2 wafers as charging monitors, and employs resist layouts emulating resist placement on product wafers. Experimental results show large differences in peak voltages and currents from fields using different resist layuots, especially at high implant energies. Comparison of results from light-field and dark-field masks indicates that light-field masks should be preferred over dark-field masks for ion implantation. The measurements obtained with this method can also be used for modeling of device charging for arbitrary combinations of device and resist layouts, and for verification of models of device charging during ion implantation.

Acknowledgment

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